KERALA TECHNOLOGICAL UNIVERSITY

(THRISSUR CLUSTER - 07)

SCHEME AND SYLLABI

of

M. TECH.

in

EMBEDDED SYSTEMS

(As on 03/09/2015)

OFFERING DEPARTMENT

ELECTRONICS &COMMUNICATION ENGINEERING

CLUSTER LEVEL GRADUATE PROGRAM COMMITTEE

1.	Dr Devdas Menon, Professor, IIT Madras,Chennai	Chairman
2	Principal, Government Engineering College Trichur, Thrissur	Convener
3	Principal, AXIS College of Engineering & Technology, East Kodaly, Murikkingal, Thrissur	Member
4	Principal, IES College of Engineering, Chittilapilly, Thrissur	Member
5	Principal, MET'S School of Engineering, Mala, Thrissur	Member
6	Principal, Royal College of Engineering & Technology, Akkikkavu, Thrissur	Member
7	Principal, Vidya Academy of Science & Technology, Thalakkottukara, Thrissur	Member
8	Principal, Thejus Engineering College, Vellarakkad, Erumappetty, Thrissur	Member
9	Principal, Universal Engineering College, Vallivattom, Konathakunnu, Thrissur	Member
10	Principal, Sahrdaya College of Engineering & Technology, Kodakara, Thrissur	Member

CERTIFICATE

This is to certify that

1. The scheme and syllabi are prepared in accordance with the regulation and guidelines issued by the KTU from time to time and also as per the decisions made in the CGPC meetings.
2. The suggestions/modifications suggested while presenting the scheme and syllabi before CGPC on 25.6.2015 have been incorporated.
3. There is no discrepancy among the soft copy in MS word format, PDF and hard copy of the syllabi submitted to the CGPC.
4. The document has been verified by all the constituent colleges.

Coordinator in charge of syllabus revision of the programme

Ms. Binet Rose Devassy
Asst.Professor,Dept.of ECE
Sahrdaya College of Engineering & Technology

Principal of the lead college

Dr.Sudha George Valavi
Principal
Sahrdaya College of Engineering & Technology

Principals of the colleges in which the programme is offered

No	Name of the college	Principal's Name	Signature
1	Sahrdaya College of Engineering & Technology	Dr.Sudha Georgre Valavi	
2	Vidya Academy of Science & Technology	Dr. Sudha Balagopalan	
3	AXIS College of Engineering & Technology	Dr.T G. Ansalam Raj	

Date: Chairman
Place:

VISION and MISSION of the Programme

VISION

To establish academic excellence and advanced research in the area of embedded systems and to provide socially responsible technocrats

MISSION

To create technically competent embedded system engineers by providing high quality education and research oriented activities to meet the future global challenges and to build individuals with the professional, ethical and societal responsibilities.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

- To develop engineers with the skills to employ hardware/software co-design in embedded systems.
- To build skilled engineers who can handle current and future industrial challenges in the field of embedded systems engineering.
- To incubate, design, develop, apply and implement products related with embedded systems.
- To pursue lifelong learning and to carry out significant research to solve challenging problems with social commitment
- To develop professional, ethical and human relationship values to perform in teams and to acquire leadership roles.

PROGRAM OUTCOMES (POs)

At the end of the course the student should be able to

- To acquire a strong foundation of embedded systems with an ability to understand, apply, analyse and synthesise the challenging engineering problems and thereby enhance their knowledge with a global outlook.
- To enhance critical thinking and solve technical issues from a firm back ground of theoretical and practical knowledge.
- To become highly proficient in Embedded hardware/Software co-design and particularly in real-time programming
- To apply appropriate research methodologies for conducting research in rapidly developing area.
- To design, conduct experiments, analyse, interpret data and demonstrate industry demanding issues using modern techniques and engineering/ IT tools
- To Develop professional and ethical attitude and become socially responsible citizens
- To practice life-long learning with commitment to improve knowledge and competence continuously.
- To demonstrate a capacity of good communication skills, self-management and teamwork, in order to achieve common goals and to develop good leadership qualities.

Scheme of M-Tech programme in Embedded Systems

SEMESTER 1:

Exam Slot	Course No:	Name	L-T-P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (Hrs)	
A	07 MA 6017	Advanced Engineering Mathematics	4-0-0	40	60	3	4
B	07 EC 6403	Advanced Embedded Processors	4-0-0	40	60	3	4
C	07 EC 6405	Advanced Digital system design	4-0-0	40	60	3	4
D	07 EC 6407	Embedded Programming	3-0-0	40	60	3	3
E	07 EC 64X9	Elective 1	3-0-0	40	60	3	3
	07GN 6001	Research Methodology	0-2-0	100			2
	07 EC 6411	Embedded Processors Laboratory	0-0-2	100	0	0	1
	07 EC 6413	Introduction to Seminar	0-0-1	0	0	1	0
TOTAL			**18 -2- 3**	**400**	**300**		**21**

SEMESTER 2:

Exam Slot	Course No:	Name	L-T-P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (Hrs)	
A	07 EC 6402	Design of Digital Signal Processing Systems	4-0-0	40	60	3	4
B	07 EC 6404	Embedded OS and RTOS	3-0-0	40	60	3	3
C	07 EC 6406	Product Design and Quality Management	3-0-0	40	60	3	3
D	07 EC 64X8	Elective 2	3-0-0	40	60	3	3
E	07 EC 64X2	Elective 3	3-0-0	40	60	3	3
	07 EC 6414	Seminar	0-0-2	100	0	0	2
	07 EC 6416	Mini Project	0-0-4	100	0	0	2
	07 EC 6418	Design of Digital Signal Processing Systems Laboratory	0-0-2	100	0	0	1
TOTAL			**16-0-8**	**500**	**300**		**21**

SEMESTER 3: CREDITS – 14

Exam Slot	Course No:	Name	L-T-P	Internal Marks	End Semester Exam		Credits
					Marks	Duration (Hrs)	
A	07 EC 74X1	Elective 4	3-0-0	40	60	3	3
B	07 EC 74X3	Elective 5	3-0-0	40	60	3	3
	07 EC 7405	Seminar	0-0-2	100	0	0	2
	07 EC 7407	Masters Research Project (Phase I)	0-0-12	50	0	0	6
TOTAL			**6-0-14**	**230**	**120**		**14**

SEMESTER 4

Course No:	Name	L-T-P	Internal Marks	End Semester Exam		Credits
				Marks	Duration (Hrs)	
07 EC 7402	Masters Research Project (Phase-II)	0-0-21	70	30	0	**12**

L – Lecture, T – Tutorial, P – Practical

Total number of credits for the PG Programme: 21+21+14+12 = 68

ELECTIVES

Elective 1	
07 EC 6409	Electronic System Design
07 EC 6419	Software Engineering
07 EC 6429	Embedded Networking

Elective II	
07 EC 6428	Embedded Applications in Power Conversion
07 EC 6438	Modern Control System Design
07 EC 6448	Information Security
Elective III	
07 EC 6412	High Speed Digital System Design
07 EC 6422	ASIC & SOC
07 EC 6432	Multimedia Compression Techniques

Elective IV	
07 EC 7401	VLSI Architecture & Design Methodologies
07 EC 7411	Electronic Instrumentation Design
07 EC 7421	Robotics & Machine Vision
Elective V	
07 EC 7403	Wireless Communication Systems
07 EC 7413	Hardware/Software Co-design in Embedded Systems
07 EC 7423	Mixed Signal System Design

SYLLABI

Core Courses

07 MA6017 ADVANCED ENGINEERING MATHEMATICS

Credits: 4-0-0: 4 **Year: 2015**

Pre-requisites: Courses on Engineering Mathematics I, II, II, IV and Digital Signal Processing

Course Objectives

- To develop the ability to apply the concepts of Matrix Theory and Linear Algebra in engineering problems.
- To understand different transforms and digital representations
- To develop the ability to apply the multidimensional transforms and wavelet transforms with engineering applications.

Syllabus

Application of matrix theory to solutions of systems of linear equations, Elementary row operations, echelon forms, invertible matrices, LU factorization. Basic ideas of vector space, Linear independence, span, basis, dimension, co-ordinate vectors, and inner product spaces. Basic ideas of transforms like Laplace Transform, Fourier Transform, Z Transform and their inverses with applications, Optical & Modulation transfer function, Random signals, Discrete Random fields, Spectral density function. Properties of orthogonal and Unitary transforms, Application of these properties to specific transforms like 1D, 2D Discrete Fourier Transforms, Discrete Cosine Transform, Hadamard, Walsh-Hadamard Transforms, Haar, Slant, KLT and SVD transforms. Introduction to wavelets and their properties, Properties of Continuous Wavelet transforms and inverse of the transform, discrete wavelet transform and orthogonal wavelet decomposition.

Course Outcome:

Students who successfully complete this course, will be able

- To develop the ability to apply the concepts of Matrix Theory and Linear Algebra in engineering problems.
- To understand different transforms and digital representations
- To develop the ability to apply the multidimensional transforms and wavelet transforms with engineering applications.

Text Books:

1. **"**Linear Algebra and its Applications**"**, David C. Lay, 3rdedition, Pearson Education (Asia) Pte. Ltd, 2005
2. Digital Arithmetic, Milos D. Ercegovac, Tomas Lang, Elsevier
3. "Fundamentals of Digital Image Processing", Anil K. Jain, PHI, New Delhi

4. Digital Signal Processing: a practical approach, Emmanuel C Ifeachor, W Barrie Jervis, Pearson Education (Singapore) Pte. Ltd., Delhi

5. Wavelet Transforms-Introduction to theory and applications, Raghuveer M.Rao and Ajit S. Bapardikar, Person Education

References:

1. Schaum's Outline for Advanced Engineering Mathematics for Engineers and Scientists , Murray R. Spiegel, MGH Book Co., New York

2. Advanced Engineering Mathematics, Erwin Kreyszing, John Wiley & Sons, NEW YORK

3. Advanced Engineering Mathematics, JAIN, R K,IYENGAR, S R K, Narosa, NEW YORK

4. Signal processing with fractals: a Wavelet - based approach, Wornell, Gregory, PH, PTR, NEW JERSEY

5. Wavelet a primer, Christian Blatter, Universities press (India) limited, Hyderabad

COURSE PLAN

07 MA 6017 ADVANCED ENGINEERING MATHEMATICS **(L-T-P : 4-0-0)** **CREDITS:4**		
MODULES	**Contact Hours**	**Sem. Exam Marks (%)**
Module I **Linear Algebra:** Linear Equations and Matrix Algebra: Fields; system of linear equations, and its solution sets; elementary row operations and echelon forms; matrix operations; invertible matrices, LU-factorization.	**9**	**15**
Module II **Vector Spaces:** Definition, subspaces**,** Linear dependence-basics-dimension-co-ordinate vectors-inner product space.	**7**	**15**
FIRST INTRENAL TEST		
Module III **Transforms and Digital Representations:** Linear Systems and Shift invariance, The Laplace Transform, Properties, The Fourier Transform, Properties of Fourier Transform, Fourier Transform of Sequence(Fourier Series) and its properties.	**10**	**15**
Module IV Z Transform and its properties, Optical & Modulation transfer function, Random signals, Discrete Random fields, Spectral density function. **Digital Arithmetic:** Fixed and Floating point representation, IEEE 754 Floating point standards, Floating point arithmetic operations .	**10**	**15**
SECOND INTRENAL TEST		
Module V **Multidimensional Transforms:** Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, 1D and 2D- DFT, DCT, Walsh, Hadamard Transform, Haar Transform, Slant Transform, KLT, SVD Transform	**10**	**20**
Module VI **Wavelet Transform-Continuous:** introduction, C-T wavelets, properties, inverse CWT. **Discrete wavelet transform and orthogonal wavelet decomposition:** examples of WT	**10**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6403 ADVANCED EMBEDDED PROCESSORS

Credits: 4-0-0: 4 **Year: 2015**

Pre-requisite:
A course on Microprocessors and microcontrollers

Course Objectives:

- To learn the architecture, programming, interfacing of certain 8 bit and 32 bit microcontrollers
- To design and develop microcontroller based embedded systems

Syllabus

Introduction to Embedded systems, Application domains and examples, Desirable features, Model of an Embedded System, General Microcontroller architecture,8051 Microcontroller, 8051 external interfacing, ARM architecture and features, Peripheral programming: using any ARM /Cortex processor chip, ARM9 Microcontroller Architecture, AT91RM9200 Architecture, Memory Controller External Bus Interface (EBI), External Memory Interface, AT91RM9200 PERIPHERALS: Interrupt Controller, System Timer , Real Time Clock , Parallel Input/output Controller

Course Outcomes:

- To understand architecture and features of typical Microcontroller.
- To learn interfacing of real world input and output devices
- To understand architecture, features and need of ARM7& ARM CORTEX processors in embedded system.
- To learn peripheral programming with ARM7& ARM CORTEX processors
- To understand architecture, features and external interfaces of ARM 9 Microcontrollers

Text books

1. Lyla B.Das: "Embedded Systems -An Integrated Approach", *Pearson Education* , India, 2012

2. Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. McKinlay, "The 8051 Microcontroller and Embedded Systems using Assembly and C", 2nd Edition, Pearson Education, 2006

Reference books

1. Lyla B. Das, The x86 Microprocessors: 8086 to Pentium, Multicores, Atom and the 8051 Microcontroller: Architecture, Programming and Interfacing, Second Edition, Pearson Education, India 2014, ISBN 978-93-325-3682

2. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide - Designing and Optimizing System Software", 2006, Elsevier

3. Ayala, Kenneth J "8051 Microcontroller - Architecture, Programming & Applications", 1st Edition, Penram International Publishing

4. Steve Furber, "ARM System-on-Chip Architecture", 2nd Edition, Pearson Education

COURSE PLAN

07 EC 6403 ADVANCED EMBEDDED PROCESSORS **(L-T-P : 4-0-0)** **CREDITS:4**		
MODULES	**Contact Hours**	**Sem. Exam Marks (%)**
Module 1 **Introduction to Embedded systems**: Application domains and examples, Desirable features, Figures of merits , Model of an Embedded System, General Microcontroller architecture ,Power on rest and brown out reset ,basic ideas of timers, counters, Real time clock , watch dog timer ,stacks, serial communications, caches ,DMA ,Pull up and pull down resistors , Memory : SRAM ,DRAM and Flash	**9**	**15**
Module 2 **The 8051 MCU**: Block diagram and architecture, Addressing Modes Programming using the 8051 instruction set, Programming the Internal peripherals of 8051, Timers, Interrupts, Serial Communication. Interfacing External peripherals: Interfacing ADCs and DACs, LCD Displays, Hex key board.	**9**	**15**
FIRST INTRENAL TEST		
Module 3 **ARM architecture:** Register set ,Modes ,Interrupt vector Table , ARM Assembly programming using the Keil RVDK tool ,ARM Instruction set ,Conditional Execution ,Arithmetic instructions, Logical Instructions, Branch instructions, Load and Store instructions, Multiple load //store instructions, Realization of stacks.	**10**	**15**
Module 4 **Peripheral programming:** using any ARM / Cortex processor chip (e.g. LPC 2148) Memory map, Peripherals on the chip ,Internal bus, PLL and memory acceleration module ,Programming the peripherals using C on Keil RVDK ,GPIO ,Timers, Interrupts PWM ,UART	**9**	**15**
SECOND INTRENAL TEST		

Module 5 **ARM9 Microcontroller Architecture**: A popular ARM9 Microcontroller from Atmel (AT91RM9200) is covered under this section . **AT91RM9200 Architecture:** Block Diagram, Features, Memory Mapping **Memory Controller (MC):** Memory Controller Block Diagram, Address Decoder, External Memory Areas, Internal Memory Mapping **External Bus Interface (EBI):** Organization of the External Bus Interface, EBI Connections to Memory Devices **External Memory Interface:** Write Access, Read Access, Wait State Management	**10**	**20**
Module 6 **AT91RM9200 PERIPHERALS:** Interrupt Controller: Normal Interrupt, Fast Interrupt, AIC System Timer (ST): Period Interval Timer (PIT), Watchdog Timer (WDT), Real-time Timer (RTT) Real Time Clock (RTC) Parallel Input/output Controller (PIO)	**9**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6405 ADVANCED DIGITAL SYSTEM DESIGN

Credits: 4-0-0: 4 **Year: 2015**

Pre-requisite:

- A course on Digital System Design.

Course Objectives:

- Thorough understanding of VHDL and modeling of digital systems using VHDL
- To be familiarize with testing and verification methodology

Syllabus:

Hardware Description Languages , Modeling, Subprograms and Packages ,VHDL synthesis, Design Examples, new developments in HDLs, Realization of SM charts,Finite State Machines: Design of finite state machines , state tables , state graphs , Reduction of state Tables State Assignment - Sequential Network Design, Designing With Programmable Devices ,Programmable LSI Techniques, Programmable Logic Devices and Field Programmable Gate Arrays - Altera Series FPGAs and Xilinx Series FPGAs, Design Issues For Testability :Introduction to Testing and Diagnosis, Fault modeling,Design for Testability: Testability -Ad hoc Design - Scan Registers and scan techniques, Test Pattern generation -Generic Off line BIST Architectures , Compression Techniques ,General aspects ,Signature Analysis

Course Outcome:

- To make the students technically competent in design and implementation using VHDL
- To expose the students to the fundamentals of sequential system design, modeling
- To enable the students to formulate and solve problems in Digital Systems design and implementation.
- To develop Digital Systems design skills.
- To introduce logics for design of Programmable Devices
- To comparatively study the classification of commercial family of Programmable
- To study on Fault identification in digital switching circuits

Text Books

1. J.Bhasker, A VHDL Primer,3/E ,PHI Learing ,2009

2. Charles L Roth, Fundamentals of Logic Design, Cenage Publishers ,India Edition,2004

3. Charles H Roth, Jr , Digital Design using VHDL , Cenage Publishers ,India Edition,2006

4. John F Wakerley, Digital Design Principles and Practice ,4th Edition , Pearson education,2006

Reference books

1. Kenneth L Short, VHDL for Engineers , Pearson Education ,2009

2. Mark Zwolinski, Digital System Design with VHDL ,Pearson Education,2004

3. MironAbramovici, Melvin Breuer, Arthur D Friedman ,Digital Systems Testing and Testable Design ,Jaico Publishing House,2005

4. Vishwani D Agrawal, Michael L Bushnel, Essentials of Electronic Testing for digital, memory mixed signal circuits,1991

COURSE PLAN

07 EC 6405 – ADVANCED DIGITAL SYSTEM DESIGN **(L-T-P : 4-0-0)** **CREDITS:4**		
MODULES	**Contact Hours**	**Sem. Exam Marks (%)**
Module 1 **Hardware Description Languages :**Introduction to VHDL - Behavioral Modeling ,Data Flow Modeling , Structural Modeling - Transport vs Inertial Delay - Simulation Deltas - Sequential Processing - Process Statement - Signal Assignment vs Variable Assignment - Sequential Statements - Data Types - Assert and report statements	**9**	**15**
Module 2 **Subprograms and Packages** - Predefined Attributes - Configurations - Subprogram Overloading - VHDL synthesis - Design Examples-,new developments in HDLs	**7**	**15**
FIRST INTRENAL TEST		
Module 3 **Finite State Machines:** Design of finite state machines –state tables – state graphs – General models for sequential networks - Derivations of State Graphs and Tables - Reduction of state Tables State Assignment - Sequential Network Design Design examples using the FSM approach –sequence detector, serial adders, multipliers, dividers. Design using ASM charts –realization of SM charts –example designs	**12**	**15**
Module 4 **Designing With Programmable Devices :**Programmable LSI Techniques - Programmable Logic Arrays - Programmable Array Logic - Sequential PLDs - Sequential Circuit Design using PLDs - Complex Programmable Logic Devices and Field Programmable Gate Arrays - Altera Series FPGAs and Xilinx Series FPGAs	**9**	**15**

SECOND INTRENAL TEST		
Module 5 **Design Issues For Testability :**Introduction to Testing and Diagnosis - Fault modeling : Logical fault models - Fault Detection and Redundancy - Fault Equivalence and Fault Location - Fault Dominance - Single stuck model - Multiple stuck model - Bridging faults	**8**	**20**
Module 6 **Design for Testability**: Testability -Ad hoc Design - Scan Registers and scan techniques -Boundary scan standards - Built in Self Test: Introduction - Test Pattern generation -Generic Off line BIST Architectures - Compression Techniques -General aspects -Signature Analysis	**9**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6407 EMBEDDED PROGRAMMING

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisite:

- A course on C programming
- A course on Microprocessors and controllers

Objectives:

- Understand the embedded programming concepts
- Familiarize with the use of C and C++ for embedded system programming

Syllabus

Introduction to Embedded C programming: Embedded programming for rabbit core, introduction to dynamic C, Basics of C++ programming, Compound data types, General concepts of object oriented programming: C++ Class overview, pointers, functions, dynamic memory allocation and de-allocation, Embedded software development tools Basics of developing for embedded systems, GNU tools

Course Outcome:

- To enable to do programming for rabbit core using dynamic C
- To know the basics of C++ programming
- To analyze software development tools for embedded systems

Text Books

1. Juan Soulié, C++ language tutorial ,ebook , 2007,online at: http://www.cplusplus.com/doc/tutorial/

2. E. Balaguruswamy, Object Oriented Programming with C++ ,Sixth Edition, TMH Publishing ,2013

3. Yedidyah Langsam, Moshe J Augenstein, Aaron M Tenenbaum, Data Structures Using C and C++ , ,Second Edition, PHI Publishers,1996

4. Lyla B.Das: ' Embedded Systems -An Integrated Approach' , Pearson Education , India,

5. Michael J Pont, Embedded C, Pearson Education ,2007

6. Embedded /Real-Time Systems: concepts, Design and Programming—The Ultimate, Prasad K.V.K.K, DREAMTECH PRESS, NEW DELHI

References books

1. Beginning J2ME-From Novice to Professional-3rd Edition , Sing Li and Jonathan Knudsen, Dreamtech Press, New Delhi

2. The Complete reference Java2, 5th Edition, Herbert Schild, TMH

3. Embedded system design using rabbit core microprocessor by Kamal Hyder, Bob Perrin 2012

COURSE PLAN

07 EC 6407 EMBEDDED PROGRAMMING **Credits: 3-0-0: 3** **Year: 2015**		
MODULES	**Contact Hours**	**Sem. Exam Marks (%)**
Module 1 **Introduction to Embedded C Programming:** Embedded programming for rabbit core, introduction to dynamic C, introduction to rabbit instruction set ,interfacing to external world, interrupts overview, multitasking, networking, soft tools **Projects**: setting up real time clock, implementing TCP/IP server	**8**	**15**
Module 2 **C++ Programming:** Structure of a program - Variables, Data types, Constants, Operators, Basic Input/ Output. Control Structures-for, if then else, while, switch. Functions - calling by reference and value.	**7**	**15**
FIRST INTERNAL EXAM		
Module 3 **Compound data types:** arrays, strings, Pointers. Programming practice using GCC or any other C compiler	**6**	**15**
Module 4 **General concepts of object oriented programming:** C++ Class overview-Class Definition Member functions, Access Control ,Class Scope , Constructors and Destructors , Inheritance , Polymorphism ,Overloading , Encapsulation ,Friend functions, this pointer, dynamic memory allocation and de-allocation-	**7**	**15**
SECOND INTERNAL TEST		
Module 5 **Applications**: Linked lists, Queues, Stacks , creation, insertion and deletion. Search algorithms ,bubble sort , insertion sort and selection sort	**6**	**20**
Module 6 **Embedded software development tools:** host and target machines, linker locator for embedded software, getting embedded software in to target system **Basics of developing for embedded systems:** embedded system initialization **GNU tools**: gcc, make files	**8**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

Elective Courses

07 EC 6409 ELECTRONIC SYSTEM DESIGN

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisite:

- A course on Linear Integrated Circuits

Objectives:

- To introduce the practical issues faced by the electronic design industry.

Syllabus

Practical Analog & Mixed Signal Circuit Design Issues and Techniques, Passive components: Understanding and interpreting data sheets and specifications of various passive and active components, Op amps: DC and AC performance, Practical Logic Circuit Design Issues and Techniques, Understanding and interpreting data sheets & specifications of various CMOS& BiCMOS family Logic devices, . CMOS/TTL Interfacing Basic design considerations for live insertion. JTAG/IEEE 1149.1 design considerations, Electromagnetic Compatibility (EMC),Designing for (EMC), EMC regulations, Cabling of Electronic Systems, Balancing & Filtering in Electronic Systems, Protection Against Electrostatic Discharges (ESD),Packaging & Enclosures of Electronic System, nature of environment and safety measures

Course Outcome

- To introduce practical analog and mixed signal circuits design issues and techniques.
- To analyze practical logic design issues
- To study and analyze Electromagnetic compatibility, cabling and grounding of electronic systems, protection against electrostatic discharges
- To analyze packaging and enclosures issues in electronic systems design.

Text books

1. Electronic Instrument Design, 1st edition; by: Kim R.Fowler; Oxford University Press.

2. Noise Reduction Techniques in Electronic Systems, 2nd edition; by: Henry W.Ott; John Wiley & Sons.

3. Digital Design Principles& Practices, 3rd edition by: John F. Wakerly; Prentice Hall International, Inc.

4. Operational Amplifiers and linear integrated circuits, 3rd edition by: Robert F. Coughlin; Prentice Hall International, Inc

5. Intuitive Analog circuit design by: Mark.T Thompson; Published by Elsevier

Reference books

1. Printed Circuit Boards - Design & Technology, 1st edition; by: W Bosshart; Tata McGraw Hill.

2. A Designer's Guide to Instrumentation Amplifiers; by: Charles Kitchin and Lew Counts; Seminar Materials @ http://www.analog.com
3. Errors and Error Budget Analysis in Instrumentation Amplifier Applications; by: Eamon Nash; Application note AN-539@ http://www.analog.com

4. Practical Analog Design Techniques; by: Adolofo Garcia and Wes Freeman; Seminar Materials@ http://www.analog.com

5. Selecting An A/D Converter; by:Larry Gaddy; Application bulletin @ http://www.Ti.com

6. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies; Application note SDAA011A@ http://www.Ti.com

7. JTAG/IEEE 1149.1 deigns considerations; Application note SCTA029@ http://www.Ti.com

8. Live Insertion; Application note SDYA012@ http://www.Ti.com

9. PCB Design Guidelines For Reduced EMI; Application note SZZA009@ http://www.Ti.com

In addition, National & International journals in the related topics, manufacturer's device data sheets and application notes are to be referred to get practical application oriented information.

COURSE PLAN

07 EC 6409 ELECTRONIC SYSTEM DESIGN **Credits: 3-0-0: 3** **Year: 2015**		
MODULES	**Hours**	**Sem. Exam Marks (%)**
Module 1 **Practical Analog & Mixed Signal Circuit Design Issues and Techniques:** **Passive components:** Understanding and interpreting data sheets and specifications of various passive and active components, non-ideal behavior of passive components,. **Op amps:** DC performance of op amps: Bias, offset and drift. AC Performance of operational amplifiers: band width, slew rate and noise. Properties of a high quality instrumentation amplifier. Design issues affecting dc accuracy & error budget analysis in instrumentation amplifier applications. Isolation amplifier basics. Active filers: design of low pass, high pass and band pass filters.	**8**	**15**
Module 2 **Practical Logic Circuit Design Issues and Techniques:** Understanding and interpreting data sheets & specifications of various CMOS& BiCMOS family Logic devices. Electrical behavior (steady state & dynamic) of CMOS& BiCMOS family logic devices.	**6**	**15**
FIRST INTERNAL TEST		
Module 3 Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies. CMOS/TTL Interfacing Basic design considerations for live insertion. JTAG/IEEE 1149.1 design considerations. Design for testability, Estimating digital system reliability. Digital circuit layout and grounding. PCB design guidelines for reduced EMI.	**7**	**15**
Module 4 **Electromagnetic Compatibility (EMC):** Designing for (EMC), EMC regulations, typical noise path, methods of noise coupling, methods of reducing interference in electronic systems. **Cabling of Electronic Systems:** Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling, magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic	**7**	**15**

fields, coaxial cable versus shielded twisted pair, ribbon cables.		
SECOND INTERNAL TEST		
Module5 **Balancing & Filtering in Electronic Systems:** Balancing, power line filtering, power supply decoupling, decoupling filters, high frequency filtering, and system bandwidth. **Protection Against Electrostatic Discharges (ESD):** Static generation, human body model, static discharge, ESD protection in equipment design, software and ESD protection, ESD versus EMC.	**7**	**20**
Module 6 **Packaging & Enclosures of Electronic System:** Effect of environmental factors on electronic system (environmental specifications), nature of environment and safety measures. Packaging's influence and its factors. **Cooling in/of Electronic System:** Heat transfer, approach to thermal management, mechanisms for cooling, operating range, basic thermal calculations, cooling choices, heat sink selection.	**7**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6419 SOFTWARE ENGINEERING

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisite:Nil

Objective:

- To help students to develop skills that will enable them to construct software of high quality – software that is reliable, easy to understand, modify and maintain

Syllabus

Software Engineering, The Software Process: Software life cycle models Software Requirements, Requirements Engineering Processes,System Models: , Architectural Design: System structuring, control models, Object-oriented Design: Objects and classes, Real-time Software Design System design, real time executives. User Interface Design:Implementation and Testing: Choice of programming languages Verification and Validation, Software Maintenance , Software Project Management ,Process Improvement

Course Outcomes:

- To Understand the Software Engineering Practice& Process Models.
- To Understand Design Engineering, Web applications and Software Project Management.
- To develop project based experience in software project management

Text books:

1. R. S. Pressman, Software Engineering, 6/e, McGraw Hill, 2002.
2. Ian Sommerville, Software Engineering, 6/e, Pearson Education Asia, 2001.
3. Shari Pfleeger, Software Engineering:Theory and Practice, Pearson Education 2001.
4. P. Jalote, An Integrated Approach to Software Engineering, Narosa, 1993.

COURSE PLAN

07 EC 6419 SOFTWARE ENGINEERING **Credits: 3-0-0: 3** **Year: 2015**		
Modules	**Hours**	**Sem. Exam Marks (%)**
Module 1 **Introduction:** What is Software Engineering, The Software Process: **Software life cycle models Software Requirements:** Functional and non-functional requirements, user requirements, system requirements, SRS.	**6**	**15**
Module 2 **Requirements Engineering Processes**: Feasibility studies, elicitation and analysis, validation, management. **System Models:** Content model, Data model, Behavioral model, Object Model	**7**	**15**
FIRST INTERNAL TEST		
Module 3 **Architectural Design:** System structuring, control models, modular decomposition, domain-specific architectures, distributed systems architecture. **Object-oriented Design:** Objects and classes, Object oriented design using UML.	**7**	**15**
Module 4 **Real-time Software Design:** System design, real time executives. Design with Reuse: Component-based development, application families, designs patterns. **User Interface Design**: Design principles, user interaction, information presentation, user support, interface evaluation.	**7**	**15**
SECOND INTERNAL TEST		
Module 5 **Implementation and Testing:** Choice of programming languages Verification and Validation, Software Testing: Unit testing, Integration Testing, Validation testing, Systems testing **Software Maintenance:** Legacy systems, software change, software re-engineering, Reverse Engineering.	**7**	**20**
Module 6 **Software Project Management:** Project planning, scheduling, risk management.. Software Cost Estimation: Productivity estimation techniques, algorithmic cost modeling, project duration and staffing. **Process Improvement:** Process and product quality, process analysis and modeling, process measurement, process CMM.	**8**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6429 EMBEDDED NETWORKING

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisite:

- A course on Communication networks

Objective:

- Learning of different embedded networking protocols.
- Familiarize various bus standards and embedded networks.

Syllabus

Embedded Communication Protocols: Embedded Networking,communication protocols: RS232 standard, RS485 ,PC Parallel port programming,USB and CAN Bus, USB bus communication, Ethernet Basics: Elements of a network , Design choices: Selecting components , Ethernet Controllers Embedded Ethernet: Exchanging messages using UDP and TCP ,Wireless Embedded Networking: Wireless sensor networks

Course Outcomes:

- To impart knowledge on
- Serial and parallel communication protocols
- Application Development using USB and CAN bus for PIC microcontrollers
- Application development using Embedded Ethernet for Rabbit processors.
- Wireless sensor network communication protocols.

Text books:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002

2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

Reference books:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.

2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003. Networking Wireless Sensors - Bhaskar Krishnamachari, Cambridge press

COURSE PLAN

07 EC 6429 - EMBEDDED NETWORKING

Credits: 3-0-0: 3 **Year: 2015**

Modules	Hours	Sem. Exam Marks (%)
Module 1 **Embedded Communication Protocols:** Embedded Networking, Introduction , Serial/Parallel Communication , **Serial communication protocols:** RS232 standard, RS485 ,Synchronous Serial Protocols ,Serial Peripheral Interface (SPI) ,Inter Integrated Circuits (I2C)	**7**	15
Module 2 **PC Parallel port programming:** ISA/PCI Bus protocols, Firewire. **USB and CAN Bus**: USB bus ,Introduction ,Speed Identification on the bus ,USB States	**6**	15
FIRST INTERNAL TEST		
Module 3 **USB bus communication**: Packets, Data flow types, Enumeration, Descriptors, PIC 18 Microcontroller USB Interface ,C Programs, CAN Bus ,Introduction , Frames ,Bit stuffing ,Types of errors, Nominal Bit Timing ,PIC microcontroller CAN Interface ,A simple application with CAN.	**6**	15
Module 4 **Ethernet Basics:** Elements of a network ,Inside Ethernet ,Building a Network: Hardware options ,Cables, Connections and network speed **Design choices:** Selecting components , Ethernet Controllers Embedded	**7**	15
SECOND INTERNAL TEST		
Module 5 **Ethernet:** Exchanging messages using UDP and TCP ,Serving web pages with Dynamic Data ,Serving web pages that respond to user Input ,Email for Embedded Systems ,Using FTP ,Keeping Devices and Network secure.	**8**	20
Module 6 **Wireless Embedded Networking:** Wireless sensor networks ,Introduction ,Applications ,Network Topology ,Localization ,Time Synchronization, Energy efficient MAC protocols ,SMAC ,Energy efficient and robust routing ,Data Centric routing.	**8**	20

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07GN6001: RESEARCH METHODOLOGY

Credits: 0-2-0 : 2 **Year : 2015**
Prerequisites : Nil

Course Objectives

The main objective of the course is to provide a familiarization with research methodology and to induct the student into the overall research process and methodologies. This course addresses:

- The scientific research process and the various steps involved
- Formulation of research problem and research design
- Thesis preparation and presentation.
- Research proposals, publications and ethics
- Important research methods in engineering

As a tutorial type course, this course is expected to be more learner centric and active involvement from the learners are expected which encourages self study and group discussions. The faculty mainly performs a facilitator's role.

Syllabus

Overview of research methodology - Research process, scientific method, research design process.
Research Problem and Design - Formulation of research task, literature review, web as a source, problem solving approaches, experimental research, and ex post facto research.
Thesis writing, reporting and presentation -Interpretation and report writing, principles of thesis writing- format of reporting, oral presentation.
Research proposals, publications and ethics - Research proposals, research paper writing, considerations in publishing, citation, plagiarism and intellectual property rights.
Research methods – Modelling and Simulation, mathematical modeling, graphs, heuristic optimization, simulation modeling, measurement design, validity, reliability, scaling, sample design, data collection methods and data analysis

Course Outcome

At the end of course, the student will be able to:

- Discuss research methodology concepts, research problems, research designs, thesis preparations, publications and research methods.

- Analyze and evaluate research works and to formulate a research problem to pursue research
- Prepare a thesis or a technical paper, and present or publish them
- Apply the various research methods followed in engineering research for formulation and design of own research problems and to utilize them in their research project.

REFERENCE BOOKS

- C. R. Kothari, Research Methodology, Methods and Techniques, New Age International Publishers
- K. N. Krishnaswamy, Appa Iyer Sivakumar, M. Mathirajan, Management Research Methodology, Integration of principles, Methods and Techniques, Pearson Education
- R. Panneerselvam, Research Methodology, PHI Learning
- Deepak Chawla, Meena Sondhi, Research Methodology–concepts & cases, Vikas Publg House
- J.W Bames, Statistical Analysis for Engineers and Scientists, McGraw Hill, N.York
- Schank Fr., Theories of Engineering Experiments, Tata Mc Graw Hill Publication.
- Willktnsion K. L, Bhandarkar P. L, Formulation of Hypothesis, Himalaya Publication.
- Fred M Kerlinger , Research Methodology
- Ranjit Kumar, Research Methodology – A step by step guide for beginners, Pearson Education
- John W Best, James V Kahan – Research in Education , PHI Learning
- Donald R. Cooper, Pamela S. Schindler, Business Research Methods, 8/e, Tata McGraw-Hill Co Ltd
- Sinha, S.C. and Dhiman, A.K., 2002. Research Methodology, Ess Ess Publications. 2 volumes
- Trochim, W.M.K., 2005. Research Methods: the concise knowledge base, Atomic Dog Publishing. 270p.
- Coley, S.M. and Scheinberg, C. A., 1990, "Proposal Writing", Sage Publications.
- Day, R.A., 1992.How to Write and Publish a Scientific Paper, Cambridge University Press.
- Fink, A., 2009. Conducting Research Literature Reviews: From the Internet to Paper. Sage Publications
- Donald H.McBurney, Research Methods, 5th Edition, Thomson Learning, ISBN:81-315-0047- 0,2006
- Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., 2002. An introduction to Research Methodology, RBSA Publishers..
- Wadehra, B.L. 2000. Law relating to patents, trademarks, copyright designs and geographical indications. Universal Law Publishing

- Carlos, C.M., 2000. Intellectual property rights, the WTO and developing countries: the TRIPS agreement and policy options. Zed Books, New York.
- Additional suitable web resources
- Guidelines related to conference and journal publications

Course Plan

07GN6001 : RESEARCH METHODOLOGY **Credits: 0-2-0 : 2** **Year : 2015**		
Modules	**Contact hours**	**Int. Exam Marks %**
Module 1 Overview of Research Methodology Research concepts – meaning – objectives – motivation - types of research –research process – criteria for good research – problems encountered by Indian researchers - scientific method - research design process – decisional research	5	10%
Module 2 Research Problem and Design Formulation of research task – literature review – methods – primary and secondary sources – web as a source – browsing tools - formulation of research problems – exploration - hypothesis generation - problem solving approaches-introduction to TRIZ(TIPS)- experimental research – principles -Laboratory experiment - experimental designs - ex post facto research - qualitative research	5	10%
FIRST INTERNAL TEST		
Module 3 Thesis writing, reporting and presentation Interpretation and report writing – techniques of interpretation – precautions in interpretation – significance of report writing – principles of thesis writing- format of reporting - different steps in report writing – layout and mechanics of research report - references – tables – figures – conclusions. oral presentation – preparation - making presentation – use of visual aids - effective communication	4	10%
Module 4 Research proposals, publications, ethics and IPR Research proposals - development and evaluation – research paper writing – layout of a research paper - journals in engineering – considerations in publishing – scientometry-impact factor- other indexing like h-index – citations - open access publication -ethical	5	10%

issues - plagiarism –software for plagiarism checking- intellectual property right- patenting case studies		
SECOND INTERNAL TEST		
Module 5 Research methods – Modelling and Simulation Modelling and Simulation – concepts of modelling – mathematical modelling - composite modelling – modelling with – ordinary differential equations – partial differential equations – graphs heuristics and heuristic optimization - simulation modelling	5	10%
Module 6 – Research Methods – Measurement, sampling and Data acquisition Measurement design – errors -validity and reliability in measurement - scaling and scale construction - sample design - sample size determination - sampling errors - data collection procedures - sources of data - data collection methods - data preparation and data analysis	4	10%
THIRD INTERNAL TEST		

Internal continuous assessment: 100 marks

Internal continuous assessment is in the form of periodical tests and assignments. There are three tests for the course (3 x 20 = 60 marks) and assignments (40 marks). The assignments can be in the form of seminar, group tasks, case studies, research work or in a suitable format as decided by the teacher. The assessment details are to be announced to students at the beginning of the semester by the teacher.

07 EC 64 11
EMBEDDED PROCESSORS LABORATORY

Maximum Marks , 100

Objectives:

Credits:1

- To explore the concepts of designing and implementing various systems using Embedded processors and microcontrollers

	Modules
1	**8-Bit 8051 Microcontroller:** **Using ASM** 1. Connect an LED to Port P1.7 of 8051 in current sinking mode. Write a program to turn ON the LED at the rate of 0.5 sec approx. Hint: Use Software Delay. 2. Modify Q1 to toggle LED on successive key press. Hint: Write key detection ISR 3. Write a program to generate a PWM waveform of 100 Hz frequency on any one of the digital I/O port. The duty cycle should vary from 0 to 100% in steps of 25%. The waveform on each step should be present for a minimum period of 500 ms. 4. Repeat the above program by providing the duty cycle from the PC using the serial port. The current duty cycle in percentage should be displayed in the LCD. **Using C** 5. Connect an LED to Port P1.7 of 8051 in current sinking mode. Write a program to turn ON the LED at the rate of 0.5 sec approx. Hint: Use Software Delay. 6. Modify the above program to toggle LED on successive key press. Hint: Write key detection ISR 7. Identify the key pressed and display the numeric value assigned to the key on the 7-Segment Display. Hint: Use the Keyboard Map for numeric values

S12 **1**	S16 **2**	S20 **3**	S24 **4**
S11 **5**	S15 **6**	S19 **7**	S23 **8**
S10 **9**	S14 **10**	S18 **11**	S22 **12**
S9 **13**	S13 **14**	S17 **15**	S21 **16**

8. Develop a 1 sec. Counter, using Timer 0 and display the count value on the 7-Segment Display
9. Generate a square wave of 100Hz using onboard DAC.
10. Read the input voltage using ADC and display it on LCD. For eg: EEH read from ADC should be displayed as Voltage = 4.76 V.
11. a) It is required to continuously monitor and control the temperature in a boiler every '1'second using the 8051 Microcontroller. The temperature has to be kept at a particular set point (50°C) with a tolerance of +/-5°C. It is assumed that the temperature is measured through an RTD sensor and is available in the range of 0V to 5V electrical signal. 0V corresponds to 0°C and 5V corresponds to 100 °C. (Use a Trimpot to apply the voltage). An ON/OFF relay connected to a Port bit is used to control the heater element. A PC is used as the monitoring station.
    b) The temperature has to be sent to the PC every '1' second by the Microcontroller.
    c) Provision should be given for changing the set point from the PC.

2

ARM 7 LPC 2148

1. Write a program to add two numbers stored in r0 and r1 registers and write the result to r2.
    a). Run the program with breakpoint and verify the result
    b). Run the program with stepping and verify the content of registers at each stage
    c). Modify the content of registers in the Tool window and re-run the program to verify the result
    d). After run, view the different formats of the registers used. Specifically, view the data in hexadecimal, decimal, octal, binary, and ASCII.
2. Write a program to multiply two numbers stored in r0 and r1 registers and write the result to r3.
    a). Put 0xFFFFFFFF and 0x80000000 into the source registers and verify the result.
    b). Modify the program to use MULS instruction in place of MUL.

	3. Write an ARM code to implement the following register swap algorithm using only two registers. a). Using arithmetic instructions b). Using logical instructions For example, take the values as a = 0xF631024C and b=0x17539ABD. 4. Write ARM assembly to perform the following array assignment in C: for (i = 0; i <= 10; i++) {a[i] = b[i] + c;} Assume that r3 contains *i*, r4 contains *c*, the starting address of array *a* is in r1, and the starting address of array *b* is in r2. 5. Write a program to find the factorial of a number using ARM assembly 6. Write a program, which sets up two parameters (r0 and r1) in THUMB state, and makes an interworking call to an ARM subroutine that adds the two parameters together and returns. 7. Modify the above program to setup the parameters in ARM state and Addition in Thumb state.
3	**ARM9 (Any ARM Based Controller)** 1. Write a program to toggle the three LED's connected to AT91RM9200 through general PIO a rate of approximately 1 second. (Use software delay). 2. Modify the above program using the system timer to generate 1-second delay. Use polling method. 3. Modify the above program using the system timer to generate 1-second delay using interrupt method. [Hint: use advanced interrupt controller]. 4. Write a program to setup a clock of 24 hour 60 minutes and 60 seconds. Use the RTC available with AT91RM9200 processor

4	**Design of a real-time data acquisition & control system using the ARM7 or ARM9 Microcontroller** . It is required to monitor and control the temperature in a boiler which ranges from 0^0C to 100^0C every **1second** using the AT91RM9200 Microcontroller. The temperature has to be kept at a set-point of 50^0C +/- 2^0 C. The temperature is measured through an RTD sensor and is transmitted through a 4-20 mA two wire transmitter. The 4-20mA is converted to 1 to 5V by 250 ohm terminating resistor. 1 to 5V is available at the analog input port. 1V corresponds to 0^0C and 5V corresponds to 100^0C. An ON/OFF relay connected to A PIO Port bit is used to control the heater element. A PC is used as the monitoring and control station. Simulate a 10 bit ADC for this application and send the data from 0V to 5V in steps of 0.1V. The same has to be repeated after reaching the maximum value of 5V. 1. The temperature has to be sent to the PC every 1 second in the following protocol format and the same has to be displayed using the LAS software in WISE-96 on the PC.

STX	MSL	CMD	S CMD	DATA_LO	DATA_HI	ETX
byte 1	Byte 2	byte 3	byte 4	byte 5	byte 6	byte 7

STX	:	Start of Text	02H
MSL	:	Message length, in bytes	
CMD	:	Command byte	90H
SCMD	:	Sub-command byte	00H (Channel no)
DATA_LO	:	Lower byte of data word	
DATA_HI	:	Upper byte of data word	
ETX	:	End of Text	03H

2. Provision should be given for receiving the set-point value of temperature from the PC, and the set point is to be framed in the above protocol format.
3. If the transmitter is switched off or if it sends invalid data, i.e, below 4mA, an error message packet similar to the above one with CMD byte set to 95H should be send to the PC, instead of the data packet.

   Hint: Use a Trimpot to apply the voltage. Use an LED to display the ON/OFF status. ON/OFF control strategy can be used for controlling the power supplied to the heater.

Software used: Keil 'C' Compiler and Assembler for 8051, ADS for ARM9

Platforms used: PC, WISE-51, WISE-196, 8051 Development Boards, ARM 7/9 Boards

Assessment procedure

i) Practical Records /outputs 40%
ii) Regular Class Viva-Voce 20%
iii) Final Test (Objective) 40%

07EC6413 INTRODUCTION TO SEMINAR

Credits: 0-0-1: 0 **Year: 2015**

Pre- requisites: Nil

Course Objectives:

- To improve the debating capability of the student to present a technical topic
- To impart training to the student to face audience and present his ideas and thus creating self esteem and courage essential for an engineer

Outline:

- Individual students are required to choose a topic of their interest and give a seminar on that topic for about 30 minutes. A committee consisting of at least three faculty members shall assess the presentation of the seminar. The committee will provide feedback to the students about the scope for improvements in communication, presentation skills and body language. Each student shall submit one copy of the report of the seminar topic.

Course Outcomes:

- The graduate will have improved the debating capability and presentation skills in any topic of his choice.

SECOND SEMESTER

Core Courses

07 EC 6402 DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS

Credits: 4-0-0: 4 **Year: 2015**

Pre-requisites:

- A course on Digital Signal Processing

Course Objectives:

- To provide basic concepts of number representations
- To understand the fundamentals of DSP architecture and to learn about pipeline issues

Course Outcomes:

- To familiarize with advanced DSP Processor
- To learn DSP programming and to know about programming tool chain
- To design and implement DSP systems for real time applications
- To understand Pipelining issues and number representations

TEXT BOOKS

1. John G Proakis, Dimitris G Manolakis Introduction to Digital Signal Processing, 1st Edition.

2. Lyla B.Das : ' Embedded Systems -An Integrated Approach' , *Pearson Education* , India, 2012.

3. On-line TI materials for the TI C6713 DSK board: http://www.ti.comUser's manuals of various fixed and floating point DSPs.

4. Naim Dahnoun Digital Signal Processing Implementation using the TMS320C6000 DSP Platform, 1st Edition.

5. R. Chassaing, Digital Signal Processing and Applications with the C6713 and C6418 DSK, John Wiley and Sons, Inc., New York, 2004.

6. Sen M. Kuo and Woon-Seng Gan.Digital Signal Processors: Architectures, Implementations, and Applications.

7. David J Defatta J, Lucas Joseph G & Hodkiss William S ;Digital Signal Processing: A System Design Approach, 1st Edition; John Wiley.

8. Andrew Bateman, Warren Yates Digital Signal Processing Design, 1st Edition.

9. A.V. Oppenheim and R.W. Schafer, Discrete-Time Signal Processing, Second edition, Prentice - Hall, Upper Saddle River, NJ, 1989.

In addition, National/ International journals in the field, manufacturers Device data sheets and application notes and research papers in journals are to be referred to get practical and application oriented information.

COURSE PLAN

07 EC 6402 DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS

Credits: 4-0-0: 4 **Year: 2015**

MODULES	Contact hours	Sem.Exam Marks;%
MODULE : 1 Introduction to a popular DSP from Texas Instruments, CPU Architecture, CPU Data Paths and Control, Timers, Interrupts	**9**	**15**
MODULE : 2 Internal Data/ Program Memory, Externl Memory Interface, pipelining,Programming : Instruction Set and Addressing Modes ,TMS 320C67X CPU Simple programming examples using C and assembly.	**9**	**15**
FIRST INTERNAL TEST		
MODULE : 3 Programming : Instruction Set and Addressing Modes ,TMS 320C67X CPU Simple programming examples using C and assembly.	**9**	**15**

MODULE : 4 Digital Signal Processing Applications: Filter Design , FIR & IIR Digital Filter Design, filter Design programs using MATLAB , Fourier Transform: DFT, FFT programs using MATLAB	**10**	**15**
SECOND INTERNAL TEST		
MODULE : 5 Real Time Implementation: Implementation of Real Time Digital filters using DSP , Implementation of FFT applications using DSP , DTMF Tone Generation and Detection	**9**	**20**
MODULE : 6 Real Time Implementation: Implementation of Real Time Digital filters using DSP , Implementation of FFT applications using DSP , DTMF Tone Generation and Detection	**10**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6404 EMBEDDED OS & RTOS

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisites:

- Knowledge of operating system (OS) basics

Course Objectives:

- Understand Theoretical background and practical knowledge of real time operating systems.
- Familiarize various Real time operating systems available and their use in embedded systems

Syllabus

Fundamentals of OS: Overview of operating system, process and threads, An overview of embedded operating system: A survey on embedded OS and RTOS, a review of POSIX standards, Introduction to FreeRTOS, Task management, Que management, Interrupt management, Resource management, Embedded Linux, GNU cross platform tool chain, embedded drivers, kernel module, porting applications, realtime linux

Course Outcomes:

- To learn OS principles of embedded systems.
- To understand the importance and basics of operating system in embedded programming.
- To understand program objectives like semaphore, pipes in Free RTOS
- Enable to handle embedded systems with Linux Os and OS porting

Text Books

1. Operting systems:A concept based approach 2E - DM Dhamdhere
2. Real time concepts of operating systems -Qing li
3. Embedded linux system design and development ,P Raghavan

4. Using the free RTOS real time kernel-Richard barry

Papers

1. A survey on operating system support for embedded system properties by Luis Fernando Friedrich

2. A survey on contemporary real time operating systems by S.Barkiyar

3. The posix family of standars by Stephen R walli

In addition, manufacturers Device data sheets, IEEE publications and application notes are to be referred to get practical and application oriented information.

COURSE PLAN

07 EC 6404 EMBEDDED OS & RTOS **Credits: 3-0-0: 3** **Year: 2015**		
Modules	**Hours**	**Sem.Exam Marks (%)**
Module1 **Fundamentals of OS**: Overview of operating system, process and threads, scheduling, memory management, virtual memory, file systems, process synchronization, dedlocks, implementation of file operations, structure of an operating system	**7**	**15**
Module2 **An overview of embedded operating system:** A survey on embedded OS and RTOS, a review of POSIX standards, defining an RTOS, the scheduler, objects, services, characteristics of an RTOS, hard realtime and soft realtime, difference between general purpose OS and RTOS, Operating system for microcontrollers	**7**	**15**

FIRST INTERNAL TEST		
Module3 **FreeRTOS**: Introduction to FreeRTOS, Task management: Task priorities, Idle task and task hook, changing priority, deleting task, The scheduling algorithm	**7**	**15**
Module 4 **Queue management**: characteristics of a que, working with large data Interrupt management: interrupt nesting,Resource management: mutex and gate keeper tasks, Memory management:- memory allocation schemes	**7**	**15**
SECOND INTERNAL TEST		
Module 5 **Embedded Linux**: Embedded linux versus desktop linux, embedded linux distributions, Architecture of embedded linux, linux kernel architecture, linux startup sequence,	**7**	**20**
Module 6 **Linux Program Development**:GNU cross platform tool chain, embedded drivers, kernel module, porting applications, realtime linux	**7**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6406 PRODUCT DESIGN & QUALITY MANAGEMENT

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisites:

Basic knowledge of economic principles

Course Objectives:

- To emphasize the concept of design this is of prior importance in manufacturing process
- Understand methods for improving the quality and reliability which are essential for economic success

Course Outcomes:

- To understand product oriented design
- To develop idea about patents, intellectual property etc
- To familiarize various statistics tool related for analyzing quality

Syllabus

Product Design and Development: Development processes, Identifying customer needs, Establishing product specifications, Concept generation, Concept selection, Product architecture, Industrial design, Design for Manufacturing, Prototyping, Robust Design, Design for Manufacturing, Prototyping, Robust Design, Patents and Intellectual property, Product Development Economics, Managing Product Development Projects., Total Quality Management : Principles and Practices: Definition of quality, Customer satisfaction and Continuous improvement,Statistical Process Control, Quality Systems, Bench Marking, Quality Function Deployment,,Product Liability, Failure Mode and Effect Analysis, Management Tools.

TEXT BOOKS

1. Total Quality Management, Second edition By: Dale H. Besterfield, Pearson Education Asia

2. Product Design & Development; Third edition By: Karl T Ulrich & Steven D Eppinger; Mc Graw Hill

In addition, relevant papers in journals & articles etc. are to be referred to get further information.

07 EC 6406 PRODUCT DESIGN & QUALITY MANAGEMENT

Credits: 3-0-0: 3 **Year: 2015**

Modules	**Hours**	**Sem Exam marks (%)**
Module 1 **Product Design and Development I:** Development processes, Identifying customer needs, Establishing product specifications, Concept generation, Concept selection	**7**	**15**
Module 2: **Product Design and Development II:** Product architecture, Industrial design, Design for Manufacturing, Prototyping, Robust Design	**7**	**15**
FIRST INTERNAL EXAM		
Module 3 **Product Design and Development III:** Design for Manufacturing, Prototyping, Robust Design, Patents and Intellectual property, Product Development Economics, Managing Product Development Projects.	**7**	**15**
Module 4 **Total Quality Management I:** Principles and Practices: Definition of quality, Customer satisfaction and Continuous improvement.	**7**	**15**
SECOND INTERNAL EXAM		
Module 5 **Total Quality Management II:** Statistical Process Control, Quality Systems, Bench Marking, Quality Function Deployment,	**7**	**20**
Module 6 **Total Quality Management III:** Product Liability, Failure Mode and Effect Analysis, Management Tools.	**7**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

Elective Courses

07 EC 6428 EMBEDDED APPLICATIONS IN POWER CONVERSION

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisites:

- A course on Power Electronics

Course Objectives:

- To Familiarize various Power Electronic conversion techniques
- To equip the students with knowledge of PWM technique

Syllabus

Power Converters, Power converter system design. , Practical Converter design considerations- Power semiconductor devices, Magnetic components: Design of high frequency transformer, design of Inductors,design of CTs, Design of controllers for Power converters,Peripheral interfacing,Designs based on dedicated gate driver ICs, Design of isolated gate drives,Design of UPS,Operation & design criteria of AC switch, DC Motor Drives: Design of adjustable speed DC motor drives, speed control of a separately excited motor, AC Motor Drives

Course Outcomes:

- To present an overview of power converters
- To learn design criteria of power converters
- To design power converters in microcontroller using PWM and interfacing
- To understand UPS design

TEXT BOOKS

1. Power Electronics; By: Mohan, Underland, Robbins; John Wiley & Sons

2. Simplified design of Switching Power supplies; By: John D Lenk; EDN series for designers.

3. Design of magnetic components for switched mode power converters; By L Umanad, S.R Bhat; Wiely Eastern ltd.

REFERENCES

1. MOSFET& IGBT Designers manual, International Rectifier

2. UPS design guide, International Rectifier

In addition, relevant papers in journals & articles etc. are to be referred to get further information

COURSE PLAN

07 EC 6428 EMBEDDED APPLICATIONS IN POWER CONVERSION

Credits: 3-0-0: 3 **Year: 2015**

MODULES	Hours	Sem Exam marks (%)
Module 1 **Power Converters:** Power converter system design. Isolated and Non-isolated dc-dc converters. Inverters with square and sinusoidal output. PWM switching, unipolar and bipolar, sine PWM	**7**	**15**
Module 2: **Practical Converter design considerations-Power semiconductor devices:** Power Diodes, BJT, MOSFET, IGBT. MOSFET & IGBT , Ratings, SOA, Switching characteristics, Gate Charge, Paralleling devices. Dos and Don'ts of using Power MOSFETs, Gate drive characteristics & requirements of power MOSFETs and IGBT modules. Design of turn on and turn off snubbers. **Magnetic components:** Design of high frequency transformer, design of Inductors, design of CTs.	**7**	**15**
FIRST INTERNAL EXAM		
Module 3 **Design of controllers for Power converters:** Micro controllers and DSP based controllers for power conversion. **Peripheral interfacing:** ADC, Keyboard, LCD display, PWM generation, Design of PWM bridge controller based on low end and high-end controllers, Interfacing of controller output to power module, Designs based on dedicated gate driver ICs, Design of isolated gate drives.	**7**	**15**
Module 4 **Design of UPS:** Online, off line UPS. Operation & design criteria of AC switch, Operation & design criteria of battery charger, operation & design criteria of inverter, active PFC circuits. Thermal design of power converters.	7	15

SECOND INTERNAL EXAM		
Module 5 **DC Motor Drives:** Design of adjustable speed DC motor drives, speed control of a separately excited motor, design of closed loop control, design chopper controlled DC motor drive, design of four quadrant chopper.	7	20
Module 6: **AC Motor Drives:** Design of 3 phase PWM VSI inverter, design of v/f control for induction Motor, design of open loop and closed loop control. Vector control of AC motors, space vectors, vector control strategy for induction motor.	7	20

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6438 MODERN CONTROL SYSTEMS DESIGN

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisites:

Signals & Systems, Control Systems

Course Objectives:

- To familiarize use of CAD tools for control system design
- To introduce soft computing concepts like Neural networks and Fuzzy logic

Syllabus

Review of continuous and discrete time system analysis, State space description of systems, Linear Quadratic (LQ) Control via Dynamic Programming, Principle of Least Squares estimation, Stochastic State Estimation, Linear Stochastic Control (Linear Quadratic Gaussian (LQG) Problem), Linear Multivariable Control, Tracking Control,CAD tools for control design, Principles of intelligent control including adaptive, learning, and self-organizing systems. Neural networks and fuzzy logic systems for feedback control.

Course Outcomes:

- To familiarize basic principles of control system and use of CAD tools for control system design
- To learn programming of control systems including CAD design.
- To understand designing intelligent control systems for fuzzy logic.

TEXT BOOKS:

1. Digital Control of Dynamic Systems; by: Franklin, Powell, Workman; Addison Wesley
2. Modern Control Design with MATLAB and SIMULINK; by: Ashish Tewari; John Wiley & Sons
3. Fuzzy Logic: Intelligence, Control, and Information ; by: John Yen, Reza Langari; Prentice Hall

REFERENCES:

1. Optimal Control Theory: An Introduction; by: Donald E. Kirk; Dover
2. Optimal Control: Linear Quadratic Methods, Anderson, B. D. O. and Moore; J. B., Prentice Hall, 1990

3. Adaptive Control, 2nd Ed., 1995; by: Astrom, K. J. and Wittenmark, B.; Addison Wesley.

4. Multivariable Feedback Design; by: J. M. Maciejowski; Addison-Wesley, 1989.

5. Control and Dynamic Systems, Neural Network Systems Techniques and Applications, Volume 7; by: Cornelius T. Leondes; Academic Press

6. Fuzzy Logic Intelligence, Control and Information; by: John Yen, Reza Langari, Pearson Education.
7. Computer Controlled Systems: Theory and Design, Third Edition; by: K. Åström, B. Wittenmark; Prentice-Hall

8. Advanced Control System Design; by: Bernard Friedland; Prentice-Hall, 1996.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

COURSE PLAN

07 EC 6438 MODERN CONTROL SYSTEMS DESIGN **Credits: 3-0-0: 3** **Year: 2015**	**Hours**	**Sem Exam marks (%)**
Modules	Hours	
Module 1 Review of continuous and discrete time system analysis by Laplace and 'z' transforms; Review of system modeling by transfer function methods; feedback, stability and sensitivity	7	15
Module 2 State space description of systems; Sampling of Systems ; Stability, robustness; Controllability and Observability, State Space Design; Pole Placement; Implementation issues ; CAD tool for control design	7	15

FIRST INTERNAL EXAM		
Module 3 **Linear Quadratic (LQ) Control via Dynamic Programming:** Review of Probability Theory, Sample Space, Random Variable, Probability Distribution and Density Functions, Correlation Function, Spectral Density,	7	15
Module 4 Principle of Least Squares estimation, Stochastic State Estimation (Kalman Filter), CAD tools for control design	5	15
SECOND INTERNAL EXAM		
Module 5 **Linear Stochastic Control (Linear Quadratic Gaussian (LQG) Problem):** Linear Multivariable Control, Tracking Control, Feed forward Control, Robust control design for multivariable systems, with uncertainties. CAD tools for control design.	8	20
Module 6 Principles of intelligent control including adaptive, learning, and self-organizing systems. Neural networks and fuzzy logic systems for feedback control. Introduction to discrete event systems and decision-making supervisory control systems.	8	20

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6448 INFORMATION SECURITY

Credits: 3-0-0: 3 **Year: 2015**

Pre - requisites:

- A course on Computer Networks

Course Objectives:

- To introduce Cryptography concepts
- To learn about system security, network security and embedded security

Syllabus

Introduction to Cryptography- OSI Security Architecture , Modern Cryptography-Secret key Cryptography, Introduction to Hash Algorithm, Introduction to Digital Signature, Introduction to PKI, System Security, Firewalls-Firewall Design, Malicious Softwares, Cyber Law and Forensics, Network Security, IP Security Overview, Transport Layer Security , Application Layer Security , Authentication Services, Embedded Security, Important Rules in Protocol Design, Miniaturization of security, Wireless Security

Course Outcomes:

- To invoke awareness about security attacks, IT acts and various encryption algorithms.
- To understand firewall design
- To incorporate security aspects to design of embedded systems

. **TEXT BOOKS**

1. Cryptography and Network Security: Principles and Practice- William Stallings
2. Practical Embedded Security: Building Secure Resource Constrained Systems - Timothy Stapko, Publisher Newnes.

REFERENCE BOOKS

1. Cryptography: Theory and Practice , 3rd Ed. SD Stinson, CRC Press.

2. Information Security for Technical Staff-SEI.

3. Guide to firewalls & network security: with intrusion detection & VPNs- HOLDEN, GREG.

4. CISSP: Certified Information Systems Security Professional Study Guide- Stewart, James Michael Et Al.56

COURSE PLAN

07 EC 6448 INFORMATION SECURITY **Credits: 3-0-0: 3** **Year: 2015**		
Modules	**Hours**	**Sem Exam marks (%)**
Module 1 **Cryptography:**Introduction to Cryptography- OSI Security Architecture **:**Security Services,Security Attacks, Security Mechanism. Introduction to Classical Cryptography.	7	15
Module 2 **Modern Cryptography-Secret key Cryptography:** DES, AES. Public key Cryptography - Diffie-Hellman, RSA, ECC. Introduction to Hash Algorithm, Introduction to Digital Signature, Introduction to PKI.	7	15
FIRST INTERNAL EXAM		
Module 3 **System Security:** Introduction, Access Control, Intrusion Detection and Prevention. **Firewalls-Firewall Design:** Principles, Firewall Characteristics, Types of Firewalls, Trusted System. .	7	15
Module 4 **Malicious Softwares :** Virus, Trojan Horse, Ad ware/ Spy ware, Worms, Logic Bomb. **Cyber Law and Forensics**: IT ACT 2000, Cyber Forensics	5	15

SECOND INTERNAL EXAM		
Module 5 **Network Security:** Introduction to Network Concepts, OSI Layers and Protocols, Network Devices, Network layer Security (IPSec) - IP Security Overview, IPSec Architecture, Authentication header, Encapsulating security Payload, Combining Security, Associations, Key management. Transport Layer Security - SSL/TLS, SET. Application Layer Security - Authentication Applications, Kerberos, X. 509 Authentication Services. E-mail Security , PGP, S/MIME.	8	20
Module 6 **Embedded Security:** Introduction, Types of Security Features , Physical, Cryptographic, Platform. Kinds of Devices- CDC, CLDC. Embedded Security Design, Keep It Simple and Stupid Principle, Modularity Is Key, Important Rules in Protocol Design, Miniaturization of security, Wireless Security, Security in WSN.	8	20

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6412 HIGH SPEED DIGITAL DESIGN

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisites:

- A course on Digital System Design

Course Objectives:

- To give the basic ideas involved in high speed digital design
- To provide knowledge of good hardware design techniques

Syllabus

Introduction to high speed digital design, Modeling of wires , Geometry and electrical properties of wires , Power distribution: Power supply network , Noise sources in digital system , power supply noise , cross talk ,Signal Interference, inter-symbol Interference, Signaling convention and circuits, simultaneous bi-directional signaling, Timing convention and synchronization, signals and events ,synchronization failure and metastability , PLL and DLL based clock aligners

Course Outcomes:

- To understand problems in high frequency system design
- To understand efficient power scheme designs for systems
- To learn troubleshooting clock problems in VLSI designs

TEXT BOOKS

1. Howard Johnson and Martin Graham, "High Speed Digital Design: A Handbook of Black Magic by",3rd Edition, (Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library), 2006

2. Stephen H. Hall, Garrett W. Hall, and James A. McCall " High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices" by , Wiley , 2007

3. Kerry Bernstein, K.M. Carrig, Christopher M. Durham, and Patrick R. Hansen "High Speed CMOS Design Styles", Springer Wiley 2006

4. Ramesh Harjani "Design of High-Speed Communication Circuits (Selected Topics in Electronics and Systems)" World Scientific Publishing Company 2006

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

07 EC 6412 HIGH SPEED DIGITAL DESIGN

Credits: 3-0-0: 3 **Year: 2015**

Modules	Hours	Sem Exam marks (%)
Module 1 **Introduction to high speed digital design:** Frequency, time and distance, capacitance and inductance effects,High speed properties of logic gates , Speed and power ,	**6**	**15**
Module 2 **Modeling of wires** Geometry and electrical properties of wires , Electrical models of wires , transmission lines ,lossless LC transmission lines , lossy LRC transmission lines , special transmission lines	**7**	**15**
FIRST INTERNAL EXAM		
Module 3 **Power distribution:** Power supply network , local power regulation , IR drops , area bonding ,On chip bypass capacitors , symbiotic bypass capacitors , power supply isolation	**7**	**15**
Module 4 **Noise sources in digital system :** power supply noise , cross talk ,Signal Interference, inter-symbol Interference, Noise Budget design, Statistical Analysis	**6**	**15**
SECOND INTERNAL EXAM		

Module 5 **Signaling convention and circuits:** Signaling modes for transmission lines , signaling over lumped transmission media , signaling over RC interconnect , driving lossy LC lines , simultaneous bi-directional signaling , terminations , transmitter and receiver circuits	**7**	**20**
Module 6 **Timing convention and synchronization:** Timing fundamentals , timing properties of clocked storage elements , signals and events , open loop timing level sensitive clocking , pipeline timing , closed loop timing , clock distribution , synchronization failure and metastability , PLL and DLL based clock aligners	**7**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6422 ASIC & SOC

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisites:

A good knowledge on digital system design

Course Objectives:

- To understand the design of ASICs and SOCs

Course Outcomes

- To provide an overview of ASIC.
- To understand library design of ASICs.
- To learn system on chip design and various optimization algorithms

Syllabus

Types of ASICs: Design flow , Economics of ASICs , ASIC cell libraries , CMOS logic cell data path logic cells, I/O cells, cell compilers
ASIC Library design: Transistors as resistors , parasitic capacitance , logical effort programmable ASIC design software: Design system , logic synthesis , half gate ASIC, ASIC Construction , Floor planning & placement , Routing
System on Chip Design Process: A canonical SoC design, SoC Design Flow , Waterfall vs Spiral, Top-Down versus Bottom-Up. Specification requirements, Types of Specifications, System Design Process, System level design issues- Soft IP vs. Hard IP, Design for Timing Closure- Logic Design Issues, Physical Design Issues; Verification Strategy, On-Chip Buses and Interfaces; Low Power, Manufacturing Test Strategies, MPSoCs. Techniques for designing MPSoCs **SoC Verification:** Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans.

TEXT BOOKS:

1. "SoC Verification-Methodology and Techniques", Prakash Rashinkar, Peter Paterson and Leena Singh. Kluwer Academic Publishers, 2001.
2. "Reuse Methodology manual for System-On-A-Chip Designs", Michael Keating, Pierre Bricaud, Kluwer Academic Publishers, second edition, 2001
3. Smith, "Application Specific Integrated Circuits", Addison-Wesley,2006

In addition, manufacturers Device data sheets and application notes are to be referred to get practicaland application oriented information.

COURSE PLAN

07 EC 6422 ASIC & SOC

Credits: 3-0-0: 3 **Year: 2015**

Modules	Hours	Sem Exam marks (%)
Module 1 **Types of ASICs:** Design flow , Economics of ASICs , ASIC cell libraries , CMOS logic cell data path logic cells, I/O cells, cell compilers.	**7**	**15**
Module 2 **ASIC Library design:** Transistors as resistors , parasitic capacitance , logical effort programmable ASIC design software: Design system , logic synthesis, half gate ASIC, ASIC Construction , Floor planning & placement , Routing	**7**	**15**
FIRST INTERNAL EXAM		
Module 3 **System on Chip Design Process:** A canonical SoC design, SoC Design Flow , Waterfall vs Spiral, Top-Down versus Bottom-Up. Specification requirements, Types of Specifications, System Design Process, System level design issues- Soft IP vs. Hard IP	**7**	**15**
Module 4 Design for Timing Closure- Logic Design Issues, Physical Design Issues; Verification Strategy, On-Chip Buses and Interfaces; Low Power, Manufacturing Test Strategies, MPSoCs. Techniques for designing MPSoCs	**7**	**15**
SECOND INTERNAL EXAM		

Module 5 **SoC Verification:** Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans.	**7**	**20**
Module 6 System level verification, Block level verification, Hardware/software co-verification, Static net list verification.	**7**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC6432 MULTIMEDIA COMPRESSION TECHNIQUES

Credits: 3-0-0: 3 **Year :2015**

Prerequisite: A basic course in information theory

Course Objectives

- To understand various text compression techniques
- To familiarize with audio compression techniques
- To equip student to work with various image compression algorithms

Syllabus

Brief history of data compression applications, Overview of information theory, Human audio, visual systems, Taxonomy of compression techniques, Source coding, rate distribution theory, vector quantization, Evaluation techniques, Text compression: Huffman coding-arithmetic coding, Shannon-Fano coding and dictionary techniques, LZW family algorithms, Audio compression: Audio compression techniquesprogressive encoding for audio-silence compression, speech compression techniques, Vocoders, Image compression, Predictive techniques, Contour based compression, Video compression techniques, Overview of Wavelet based compression and DVI technology- Motion video compression, DVI real time compression

Course Outcomes

- Understand the importance of data, audio and image compression
- Implement various audio and image compression algorithms

Text books:

1. SayoodKhaleed, Introduction to data compression, Morgan Kauffman,London,1995
2. Mark Nelson, Dta compression book, BPB Publishers, New Delhi, 1998
3. Watkinson,J. Compression in video and audio, Focal press,London.1995

Jan Vozer, Video compression for multimedia, AP profes, NewYork,1995.

COURSE PLAN

07 EC6432 MULTIMEDIA COMPRESSION TECHNIQUES (L-T-P : 3-0-0) CREDITS:3		
MODULES	**Contact hours**	**Sem.Exam Marks;%**
Module 1 Introduction: Brief history of data compression applications-Overview of information theory- redundancy- Human audio, visual systems, Taxonomy of compression techniques	**7**	**15**
Module 2 Source coding, source models- scalar quantization theory- rate distribution theory- vector quantization- structure of quantizer's- Evaluation techniques-error analysis and methodologies	**7**	**15**
FIRST INTERNAL TEST		
Module 3 Text compression: Compact techniques-Huffman coding-arithmetic coding-Shannon-Fano coding and dictionary techniques-LZW family algorithms- Entropy measures of performance-Quality measures	**7**	**15**
Module 4 Audio compression: Audio compression techniques-frequency domain and filtering-basic sub-band coding-application to speech coding-G.722-application to audio coding-MPEG audio, progressive encoding for audio-silence compression- speech compression techniques-Vocoders	**7**	**15**
SECOND INTERNAL TEST		
Module 5 Image compression: Predictive techniques-PCM, DPCM, DM. Contour based compression-quad trees, EPIC, SPIHT, Transform coding, JPEG, JPEG-2000, JBIG	**7**	**20**
Module 6 Video compression: Video signal representation- Video compression techniques-MPEG, Motion estimation techniques-H.261. Overview of Wavelet based compression and DVI technology- Motion video compression- PLV performance- DVI real time compression	**7**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 6414 :SEMINAR

Credits: 0-0-2: 2 **Year: 2015**

Prerequisite: Nil

Course Objectives : This course is intended for

- Increasing the breadth of knowledge
- Enhancing the ability of self study
- Improving presentation and communication skills
- Augmenting the skill of Technical Report Writing.

Course Outcomes:

The graduate will have acquired

- Debating capability and presentation skills in a technical topic of his interest.
- Knowledge about contemporary issues and research opportunities
- Capacity to communicate effectively and professionally in both verbal and written forms
- Capability for self education and lifelong learning

Outline and Evaluation procedure:

Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 30 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students. Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.

Internal continuous assessment : 100 marks

Marks for the report: 30%

Presentation: 40%

Ability to answer questions on the topic: 30%

07EC6416 MINI PROJECT

Credits: 0-0-4: 2 **Year: 2015**

Prerequisite: Nil

Course Objectives:

- To practice the steps involved for the selection, execution, and reporting of the project

Outline and Evaluation procedure:

Individual students are required to choose a topic of their interest in the field of Embedded systems. The subject content of the mini project shall be from emerging / thrust areas, topics of current relevance having research aspects. The final evaluation of mini project will be carried out by a committee consisting of three faculty members from the department. The students should bring the report duly authenticated by the respective guide. Students individually will present their work before the committee. The report complete in all respects should be submitted to the Head of the department.

Course Outcomes:

- The graduate will have acquired skills to select and execute projects.
- The graduate will have acquired technical report writing skills.

Internal continuous assessment: 100 marks

The distribution of marks for the mini project is as follows.

Report – 20%

Demonstration and presentation – 50%,

Results -30%

07 EC 6418
DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS LABORATORY

Credits: 0-0-2: 1 **Year: 2015**

Course Objective

- Acquire sufficient expertise in simulating the systems using MATLAB or any other equivalent tool.

Course Outcomes

- Enables the students to explore the concepts of designing and implementing various systems using DSP kits.
- Upon completion, the students will be able to design enlisted experiments and implement using hardware

Platforms used: PC, TMS320C6713 Starter Kits, Xilinx/ Altera FPGA Kits

REFERENCES:

1. Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform, 1st Edition; by: Naim Dahnoun

2. DSP Applications using 'C' and the TMS320C6X DSK, 1st Edition; by: Rulph Chassaing

3. Digital Signal Processing with Filed Programmable Gate Arrays: 2nd Edition, by: U. Meyer , Base, Springer

4. Digital Signal Processing: A System Design Approach, 1st Edition; by: David J Defatta J, Lucas Joseph G & Hodkiss William S; John Wiley

5. Real - Time Digital Signal Processing: Implementations, Applications, and Experiments with the TMS320C55X, Kuo, Sen M, Lee, Bob H, John Wiley & Sons Ltd.
6. Digital Signal Processing , Architecture, Programming and Applications, by: B.Venkataramani & M.Bhaskar; Tata McGraw Hill

7. Digital Signal Processing - A Student Guide, 1st Edition by T.J. Terrel and Lik-Kwan Shark; Macmillan Press; Ltd.

In addition, National/ International journals in the field, manufacturers Device data sheets and application notes and research papers in journals are to be referred to get practical and application oriented information

07 EC 6418
DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS LABORATORY

Credits: 0-0-2: 1 **Year: 2015**

Modules

DSP Fundamentals using TMS320C6713

1. Write a program to implement convolution of x(n) with h(n) using linear convolution and verify the result y(n) as below.
   x(n) = [1,1,1,1,0.5,0.5,0.5,0.5] , h(n) = [0.3,0.25,0.2,0.15,0.1,0.05] and y(n) == [0.3,0.55,0.75,0.9,0.85,0.775,0.675,0.6,0.4.0.25,0.15,0.075,0.025]
2. Write a program for circular convolution of the following inputs x(n) and h(n) and Verify the output y(n) as given below:
   x(n) = [1,1,1,2,1,1] , h(n) = [1,1,2,1] and y(n) = [6,5,5,6,6,7]
3. Implement an 8-point DFT for the inputs x(n) and verify the result as X(K). Where, x(n) = [1,1,1,1,1,1,0,0] and X(K) = [6,-0.707-j1.707,1-j,0.707+j0.293,0,0.707-j0.293,1+j,-0.707+j1.707].
4. Find IDFT of the sequence X(K) = [11110000]. Verify that x (n) = [0.5,0.125+j0.30175, 0,0.125+j0.05175, 0,0.125-j0.05175, 0,0.125-j0.30175]
5. Generate the following waveforms using the Codec on DSK and verify the outputs for different frequencies (1 KHz, 2KHz etc.)
   a) Sine wave
   b) Square wave
6. Tone Generation using the serial port and Codec of the DSK.
   a) Generate a simple tone of a fixed frequency (1 KHz).
   b) Generate multiple tones using Codec at frequencies starting from 300Hz to 3 KHz with an increment of 100Hz each tone for duration of 1second using timer interrupt.
7. Transfer an array of numbers from PC to DSP and get back the Bit Reversed form using Probe point.

Digital Signal Processing Algorithms

1. Design an FIR Low pass Filter with following specification. fp = 1500Hz, fs = 2000Hz, Pass band attenuation = 0.01dB, Stop band attenuation = 40dB and Fs = 8000 Hz using Kaiser window.
2. Write programs for DFT, FFT using Matlab

Digital Signal Processing Application

1. Real-time Implementation of FIR filters
    a) Generate the filter coefficients using Kaiser Window for a low pass FIR filter for the specification as given in experiment 1 of module 2.
    b) Apply an input signal through a Codec; implement the filter on TMS320C6713 DSK. Vary the input signal frequency and observe the output on an Oscilloscope.
    c) Repeat the filter for Band pass and High pass.
    d) Repeat the same with hamming window.
2. Fourier Transform-Perform FFT analysis for the signal input through the Codec and display the input signal as well as the FFT output on PC using Probe point facility. Perform FFT operation for 16, 32 and 64-point FFT. Compute the power spectrum $X(K) * X(K) = |X(K)|^2 = Xreal^2 + Ximag^2$ and plot the same in PC.
3. DTMF Tone Generation and Detection and its implementation. Generate DTMF Tones. Detect the DTMF tone input trough the Codec. Implement the program with Geortzel algorithm
4. Implementation of Speech processing applications

Current trends in Digital Signal Processor (any two)

1. Implementation of Serial/Parallel Convolver using FPGAs
2. Implementation of a length four FIR filter using VHDL
3. Designing a four-tap Direct FIR filter using VHDL
4. Cooley - Tukey FFT Algorithm implementation using FPGA

Assessment procedure

i) Practical Records /outputs 40%
ii) Regular Class Viva-Voce 20%
iii) Final Test (Objective) 40%

THIRD SEMESTER

Elective Courses

07 EC 7401 - VLSI ARCHITECTURE AND DESIGN METHODOLOGIES

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisite:

- A course on Digital System Design.

Course Objectives:

- To make the student learn to understand VLSI design methodologies and ASIC.

Course Outcome:

- To understand VLSI design methodologies
- To give an insight to the students about the significance of CMOS technology and fabrication process.
- To introduce High speed VLSI techniques
- To teach the importance and architectural features of programmable logic devices
- To introduce the ASIC construction and design algorithms

Syllabus

Overview of digital VLSI design methodologies , Trends in IC Technology , Design of logic circuits,Synthesis of multiple output combinational logic circuits , Analog vlsi and high speed vlsi, realization of neural networks and switched capacitor filters , Sub-micron technology and Gas VLSI Technology., Programmable ASICs, PREP bench marks , Actel ACT , Xilinx LCA , Altera flex , Altera MAX DC & AC inputs and outputs , Clock and power inputs , Xilinx I/O block, Programmable ASIC design software: Actel ACT , Xilinux LCA , Xilinux EPLD , Altera MAX 5000 and 7000 , Altera MAX 9000 , design systems , logic synthesis

Text books

1. William I.Fletcher, "An Engineering Approach to Digital Design", Prentice Hall of India.

2. AmarMukharjee,"Introduction to NMOS and CMOS VLSI System Design", Prentice Hall, 1986.

3. M.J.S. Smith, "Application , specific integrates circuits", Addison Wesley Longman Inc. 1997.

4. Frederick J.Hill and Gerald R.Peterson, "Computer Aided Logical Design with emphasis on VLSI".

COURSE PLAN

07 EC 7401 - VLSI ARCHITECTURE AND DESIGN METHODOLOGIES **Credits: 3-0-0: 3** **Year: 2015**		
Modules	**Hours**	**Sem. Exam Marks (%)**
Module1 **Introduction:** Overview of digital VLSI design methodologies , Trends in IC Technology , Advanced Boolean algebra , Shannon's expansion theorem , Consensus theorem , Octal designation- Run measure , Buffer gates - Gate expander , Reed Muller expansion	**7**	**15**
Module2 **Design of logic circuits** Synthesis of multiple output combinational logic circuits by product map method , Design of static hazard free, dynamic hazard free logic circuits	**7**	**15**
FIRST INTERNAL TEST		
Module3 **Analog vlsi and high speed vlsi:** Introduction to analog VLSI , realization of neural networks and switched capacitor filters , Sub-micron technology and Gas VLSI Technology.	**7**	**15**
Module4 **Programmable ASICs:** Anti fuse , static RAM , EPROM and technology , PREP bench marks , Actel ACT , Xilinx LCA , Altera flex , Altera MAX DC & AC inputs and outputs , Clock and power inputs , Xilinx I/O blocks.	**7**	**15**

SECOND INTERNAL TEST		
Module 5 **Programmable ASIC design software:** Actel ACT , Xilinux LCA , Xilinux EPLD , Altera MAX 5000 and 7000 , Altera MAX 9000	**7**	**20**
Module 6 **Synthesis :**design systems ,logic synthesis , half gate , schematic entry , Low level design language , PLA tools , EDIF , CFI design representation.	**7**	**20**

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 7411 - ELECTRONIC INSTRUMENTATION DESIGN

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisite:

Analog and mixed signal design

Objective:

To understand the operation of typical instrumentation systems Identify the various nethods of signal transmission

Outcomes:

- Be able to describe and model different electrical transducers
- Design an optimum amplifier for a transducer
- Design signal conditioning circuits for limiting, filtering, and waveform shaping
- Specify the performance required from A/D and D/A converters in a design.
- To know about smart sensors and its data acquisition

Syllabus

Architecture of Instrumentation scheme,Static and dynamic characteristics, Electrical I/O characteristics of sensors/transducers for measurement ,Signal conditioning, Operational and Instrumentation Amplifiers. Instrumentation amplifiers , Analog Signal Acquisition, Conditioning and Processing, Input grounding, Shielding, and Termination Practice, Devicesfor Data Conversion , Signal Recovery and Interpolation ConversionSystem Design with Computer , Introduction to smart sensors, Sensor design, Smart sensor Buses and Interface circuits

Text books

1. Measurement and Instrumentation Principles, by: Alan S. Morris, Butterworth-Heinemann
2. Advanced Instrumentation and Computer I/O Design, by: Patrick H. Garrett, IEEE Press
3. Data Acquisition and Signal Processing for Smart Sensors, by: Nikolay V. Kirianaki et al., John Wiley & Sons
4. Microsensors MEMS and Smart Devices, by: Julian W. Gardner, Vijay K. Varadan, et al., John Wiley & Sons

References

1. Industrial Instrumentation Principles and Design, 1st edition; by:Tattamangalam. R.Padmanabhan, Springer Verlag.

2. Measurement Systems Application and Design, by: Ernest O. Doebelin, McGraw-Hill Science/Engineering/Math

3. Handbook of Transducers, 1stedition; by: Harry N.Norton, Prentice Hall.

4. Advances in Distributed Sensor Technology; by: S.S.Iyengar, L.Prasad, Hla Min; Prentice Hall PTR

5. Standard Recommended Practises for Instrumentation & Control, Vol 1-3,11thedition; Instrument Society of America.

6. Microsensors: Principles and Applications; by: Gardner, J W, Wiley (1994)

7. Measurement Systems, Application and Design, 4th edition; by: Ernest O.Doebelin, McGraw- Hill.

8. Practical Design Techniques For Sensor Signal Conditioning; Seminar Materials@ http://www.analog.com

9. Data Acquisition Fundamentals; Application Note AN007 @ http://www.ni.com

10. Measurement Systems And Sensors (Hardcover), By: Waldemar Nawrocki , Artech House Publishers

11. Introduction to Instrumentation and Measurements, by: Robert B. Northrop, CRC; 2 edition

12. Microtransducer CAD: Physical and Computational Aspects (Computational Microelectronics) (Hardcover), by: Arokia Nathan (Author), Henry Baltes (Author), Springer

In addition National & International journals in the related topics shall be referred. Manufacturer's device data sheets and application notes are to be referred to get practical application oriented information.

COURSE PLAN

07 EC 7411 - ELECTRONIC INSTRUMENTATION DESIGN		
Credits: 3-0-0: 3	**Year: 2015**	
Modules	**Hours**	**Sem. Exam Marks (%)**
Module 1 **Architecture of Instrumentation scheme:** Static and dynamic characteristics, errors, standards and calibration. Principle and design of various active and passive transducers. Introduction to semiconductor sensors and its applications.	7	15
Module 2 Electrical I/O characteristics of sensors/transducers for measurement of temperature, flow, level, pressure, position and motion. Specifications and selection of sensors/transducers for measurement of temperature, flow, level, pressure, position and motion.	7	15
FIRST INTERNAL TEST		
.**Module3** Amplification, attenuation, isolation, multiplexing, filtering, linearization, compensation, simultaneous sampling & transducer excitation Operational and Instrumentation Amplifiers. Instrumentation amplifiers and Error Budgets, Noise in Low level Amplification.	7	15
Module 4 Analog Signal Acquisition, Conditioning and Processing, Input grounding, Shielding and Termination Practice. Signal conditioning Error Analysis. DC, Sinusoidal and Harmonic Signal Conditioning, Analog Signal Processing,	7	15
SECOND INTERNAL TEST		

Module5 Devices for Data Conversion , Analog Multiplexers, Sample , Holds, D/A and A/D Sampled Data, Inter sample Error and Interpolation, Aliasing of Signal and Noise, Inter sample and Aperture Error, Signal Recovery and Interpolation Conversion System Design with Computer , Assisted Analysis, System Design Considerations, Computer Assisted Interface Analysis Software	7	20
Module 6 Introduction to smart sensors, Voltage to Frequency Converters and Frequency to Code converters, Data Acquisition methods for multi Channel sensor systems, Smart Sensor design, Smart sensor Buses and Interface circuits.	7	20

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 7421 - ROBOTICS AND MACHINE VISION

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisite:

- A course on Digital Image Processing

Course Objectives:

- To study basics of machine vision concepts applicable to robotics.

Course Outcome:

- To analyze kinematics and positional control of articulated manipulators
- To study design techniques for controlling mechanical systems;
- To apply image processing techniques and transforms
- To apply edge enhancement techniques and image analysis

Syllabus

Industrial Robots: Basic Concepts of Robotics, Classification and Structure of Robotic Systems Kinematics Analysis and Coordinate Transformations, Industrial Applications of RobotsPrinciples of Machine Vision, Image acquisition , Illumination, Image formation and Focusing, Image Detection , Introduction, Types of Cameras; Image Processing and Presentation Image Processing Techniques: Fundamental Concepts of Image Processing,. Basic Machine Vision Processing Operators , Transformations:Monadic one Point Transformations: Dyadic Two Point ransformations ,Image Addition, Image Subtracting, Image Multiplication; Convolution and Spacial Transformation, Edge Enhancement Techniques and Image Analysis,Image Analysis

Text books:

1. Machine Vision and Digital Image Processing, by Louis J. Galbiati, Jr. Prentice Hall, Englewood Cliffs, New Jersy.

2. Robotics for Engineers, By, Yoram Koren, McGraw Hill.
3. Robotics and Image Processing , an Introduction, by Janakiraman P. A., Tata McGraw Hill, New Delhi

4. Digital Image Processing and Computer Vision by Robert J.Schalkoff, John Wiley & Sons Inc.

References:

1. Industrial Robotics , Technology, Programming and Applications, by Mikell P. Groover, Mitchell Wein, Roger N. Nagel and Nicholas G. Odlrey, McGraw Hill International Edistion.

2. Handbook Of Image Processing Operators by Klette, Reinhard & Zamperoni, Piero; John Wiley & Sons Inc

3. Image Processing, Analysis And Machine Vision by Sonka, Milan Et Al

4. Industrial Robotics by Hodges, Bernard, Jaico Publishing House, Delhi

5. Introductory Computer Visiona dn Image Processing by Adrian Low, McGraw Hill International Editions.

6. In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

COURSE PLAN

07 EC 7421 - ROBOTICS AND MACHINE VISION **Credits: 3-0-0: 3** **Year: 2015**		
Modules	Hours	**Sem. Exam Marks (%)**
Module 1 **Industrial Robots:** Basic Concepts of Robotics, Classification and Structure of Robotic Systems Kinematics Analysis and Coordinate Transformations, Industrial Applications of Robots, and Programming	7	15
Module 2 **Introduction Machine Vision:** Principles of Machine Vision, Vision and factory automation, Human Vision Vs. Machine Vision, Economic Considerations, Machine Vision	7	15
FIRST INTERNAL TEST		
Module 3 **System Overview** ;- Image acquisition , Illumination, Image formation and	7	15

Focusing, Image Detection , Introduction, Types of Cameras; Image Processing and Presentation		
Module 4 **Image Processing Techniques:** Fundamental Concepts of Image Processing, Pixel, Pixel Location. Gray Scale, Quantizing Error and Measurement Error and Histograms. Basic Machine Vision Processing Operators ,	7	15
SECOND INTERNAL TEST		
Module 5 **Transformations**:Monadic one Point Transformations: Identity operator, Inverse Operator, Threshold operator and other operators viz: Inverted Threshold operator, Binary Threshold operator, Inverted Binary Threshold Operator, Gray Scale Threshold and Inverted Gray Scale Threshold Operators; Dyadic Two Point ransformations ,Image Addition, Image Subtracting, Image Multiplication; Convolution and Spacial Transformations	7	20
Module 6 **Edge Enhancement Techniques and Image Analysis:** Introduction, Digital Filters , Low pass and High Pass filters; Edge Engancement Operators , Laplacian, Roberts Gradient, Sobel and other Local operators. Image Analysis: Thresholding, Pattern Matching and Edge Detection, Back-Propagation Algorithm	7	20

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 7403 - WIRELESS COMMUNICATION SYSTEMS

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisite:

- A course on Antenna and Propagation, Digital Communication

Course Objectives:

- To introduce and study established and emerging areas of wireless communication systems

Syllabus

Introduction to Wireless Systems: Evolution of Wireless Communication, Modulation techniques, Frequencies used and licensing, Spread Spectrum Technologies, Multiple Access Techniques for Wireless Communications, Satellite-based wireless Communications, 1st, 2nd, 3rd and 4th Generation Cellular Systems, GSM, CDMA GPRS, EDGE, EVDO CDMA2000, UMTS, WCDMA, LTE, Wireless Web connectivity, Mobile IP, Wireless in local loop, Antenna Basics, Cellular and PCS Antennas, MIMO, Mobile Radio Propagation: Free-space propagation model, Wireless Personal Area Networks, Sensor Networks, Interfacing problems and co-existence strategies in Sensor Networks

Course Outcome:

- To introduce the concepts of wireless / mobile communication using cellular environment
- To provide the student with an understanding of advanced multiple access techniques
- To provide the student with an understanding of diversity reception techniques
- To enable to understand digital cellular systems
- To introduce various wireless network systems and standards

Text books

1. Wireless Communications , Principles and Practice; by Theodore S Rappaport, Pearson Education Pte. Ltd., Delhi

2. Wireless Communication Technology; By: Blake, Roy; Delmar, New York.

3. Wireless Communications and Networking; By: Stallings, William; Pearson Education Pte. Ltd., Delhi

4. Bluetooth Revealed; By: Miller, Brent A, Bisdikian, Chatschik; Addison Wesley Longman Pte Ltd., Delhi

References

1. Mobile and Personal Communications Services and Systems; 1st Edition; By: Raj Pandya; PHI, New Delhi

2. Fundamentals of Wireless Communication by Tse David and Viswanath Pramod, Cambridge University press, Cambridge

3. Mobile Communications; By: Schiller, Jochen H; Addison Wesley Longman Pte Ltd., Delhi

4. 3G Networks: Architecture, protocols and procedures based on 3GPP specifications for UMTS WCDMA networks, By Kasera, Sumit, Narang, and Nishit, TATA MGH, New Delhi

5. Mobile Communications Engineering; Theory and Applications, By: Lee, William C Y; MGH, New York

6. Wireless Sensor Networks: information processing by approach, ZHAO, FENG, GUIBAS and LEONIDAS J, ELSEVIER, New Delhi

7. Wireless Network Evolution: 2G to 3G by GARG, VIJAY K, Pearson Education (Singapore) Pte. ltd., Delhi

In addition, manufacturers Device data sheets, IEEE publications and application notes are to be referred to get practical and application oriented information.

COURSE PLAN

07 EC 7403 - WIRELESS COMMUNICATION SYSTEMS		
Credits: 3-0-0: 3	**Year: 2015**	
Modules	Hours	**Sem. Exam Marks (%)**
Module 1 **Introduction to Wireless Systems:** Evolution of Wireless Communication, Cordless Telephones, Paging and messaging systems, Cellular Systems, Analog and Digital Cellular, Modulation techniques	7	15
, **Module 2** Frequencies used and licensing, Spread Spectrum Technologies, Multiple Access Techniques for Wireless Communications, Satellite-based wireless Communications,GPS	7	15
FIRST INTERNAL TEST		
Module 3 **Cellular Systems:** Cellular carriers and Frequencies, Channel allocation, Cell coverage, Cell Splitting, Microcells, Picocells, Handoff, 1st, 2nd, 3rd and 4th Generation Cellular Systems, GSM, CDMA GPRS, EDGE, EVDO CDMA2000, UMTS, WCDMA, LTE, Wireless Web connectivity, Mobile IP, Wireless in local loop (WLL)	7	15
Module 4 **Radio propagation in Mobile Systems:** Antenna Basics, Cellular and PCS Antennas, MIMO, Mobile Radio Propagation: Free-space propagation model, Two-Ray Model, Outdoor and indoor propagation models,Fading Channels, Raleigh and Ricean Distribution.	7	15
SECOND INTERNAL TEST		
Module 5- Wireless LANs and PANs: Wireless LANs: 802.11,802.11a/b/g, 802.16-WiMAX, UWB Communications , Wireless Personal Area Networks, BlueTooth, BlueTooth Protocol Architecture, IEEE 802.15 standards, ZigBee,	7	20

Module6 Sensor Networks, Interfacing problems and co-existence strategies in Sensor Networks, MAC and Routing protocols in Sensor Networks.	7	20

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 7413 - HARDWARE/SOFTWARE CO-DESIGN IN EMBEDDED SYSTEM

Credits: 3-0-0: 3 **Year: 2015**

Pre-requisite:

- A course on Embedded system basics

Course Objectives:

- The course will cover system level design of embedded system with top-down design approach.
- The students will learn various design steps starting from system specifications to hardware/software implementation and will experience process optimization while considering various design decisions

Syllabus

Introduction to embedded hardware and software , Interrupt routines in an RTOS environment , System modeling with hardware/software partitioning : Embedded systems, Hardware/Software Co-Design, Co-Design for System Specification and modeling,Design:- Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, hardware/software co-synthesis: The Co-Synthesis Problem, Distributed System Co-Synthesis, Concurrent process models and hardware software co-design : Modes of operation ,Models,Communication among process ,Synchronization among process , Implementation , Data Flow model. Design technology,Design Process Model.

Course outcomeObjectives:

- To underastand the Fundamentals on design attributes of functional units of a Processor
- To analyse on Hardware software portioning in system design
- To understand intra & Inter processor Communications
- To study strategies for processor Communications
- To study Co-Designs

Text books

1. David. E. Simon, “An Embedded Software Primer”, Pearson Education, 2001.

2. Tammy Noergaard, ”Embedded System Architecture, A comprehensive Guide for Engineers and Programmers”, Elsevier, 2006

3. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.

4. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & sons, 2002

References

1. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.

2. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.

3. Jorgen Staunstrup, Wayne Wolf, “Harware/Software Co-Design:Principles and Practice”, Kluwer Academic Pub, 1997.

4. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design” Kaufmann Publishers, 2001.

COURSE PLAN

07 EC 7413 - HARDWARE/SOFTWARE CO-DESIGN IN EMBEDDED SYSTEM **Credits: 3-0-0: 3** **Year: 2015**		
Modules	**Hours**	**Sem. Exam Marks (%)**
Module 1 **Introduction to embedded hardware and software :**Terminology , Gates , Timing diagram , Memory , Microprocessor buses , Direct memory access , Interrupts , Built interrupts , Interrupts basis , Shared data problems , interrupt latency - Embedded system evolution trends , Interrupt routines in an RTOS environment .	**7**	15
Module 2 **System modeling with hardware/software partitioning :** Embedded systems, Hardware/Software Co-Design, Co-Design for System Specification and modeling- Single-processor Architectures & Multi-Processor Architectures, comparison of CoDesign Approaches, Models of computation	**7**	15
FIRST INTERNAL TEST		
Module 3 **Design:-**Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modeling, Formulation of the HW/SW scheduling, Optimization	**7**	**15**
Module 4 **hardware/software co-synthesis:** The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.	**7**	15
SECOND INTERNAL TEST		

Module 5 **Concurrent process models and hardware software co-design :** Modes of operation , Finite state machines , Models , HCFSL and state charts language, state machine models , Concurrent process model , Concurrent process	**7**	20
Module 6 **Models:-**Communication among process ,Synchronization among process , Implementation , Data Flow model. Design technology, Automation synthesis, Hardware software co-simulation, IP cores, Design Process Model.	**7**	20

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 7423 MIXED SIGNAL SYSTEM DESIGN

Credits: 3-0-0: 3 **Year: 2015**

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Pre-requisite:

Analog and mixed signal design

Objective:

To understand mixed signal design methodology

Syllabus

Physics of electronic devices CMOS Inverter AC and DC Characteristics, Analog Signal ProcessingDigital Sub Circuits: CMOS Logic implementation basics- Logic gates and Flip flops –Transmission Gates, TG based implementation of multiplexers, de-multiplexers, encoders, decoders, Comparator, Parity generator,Memory elements, Analog Sub circuits: Operational Amplifier, Inverting and Non-inverting configuration Differential Ideal amplifier basics, VCO, PLL, Comparator characteristics, two stage open loop comparator ,Switched capacitor fundamentals, Switched capacitor amplifier, Digital to Analog Data Converters : Static &Dynamic Charatersitics, Analog to Digital Data Converters: Static &Dynamic Characteristics,Concept of over sampling

Course Outcomes:

1. To review CMOS basics and digital circuit design.
2. To learn to design and analyze analog circuits like VCO, PLL.
3. To learn how to design and analyze switched capacitor circuit.
4. To learn how to design and analyze mixed signal circuits.
5. To figure out various factors that go into the design of mixed signal circuits.
6. To learn how to design and analyze DAC, ADC and data converters.

Text books

1. CMOS Analog Circuit Design, 2nd edition; by: Allen, Phillip E, Holberg , Douglas R, Oxford University Press, (Indian Edition)

2. D A John, Ken Martin, Analog Integrated Circuit Design, 1st Edition, John Wiley

3. Ken Martin, Digital Integrated Circuit Design, John Wiley

4. Gray Paul R, Meyer, Robert G, Analysis and Design of Analog Integrated Circuits, 3rd edition, John Wiley & Sons.

5. Sedra & Smith, Microelectronics Circuits, 5th Edition, Oxford University Press, (Indian Edition)

6. Jan M. Rabaey, Anantha Chadrakasan, B. Nikolic ,Digital Integrated Circuits , A Design Perspective 2nd Edition, Prentice Hall of India (Eastern Economy Edition).

7. Sung-Mo Kang**,** Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis & Design,2nd Ed,Tata McGraw Hill

COURSE PLAN

07 EC 7423 MIXED SIGNAL SYSTEM DESIGN **Credits: 3-0-0: 3** **Year: 2015**		
Modules	**Hours**	**Sem. Exam Marks (%)**
Module 1 **Introduction**: PN Junctions, Bipolar Vs Unipolar Devices, MOS Transistor operation, MOS Transistor as a Switch, NMOS ,PMOS and CMOS Switches, CMOS Inverter AC and DC Characteristics, Analog Signal Processing	**7**	15
Module 2 **Digital Sub Circuits**: CMOS Logic implementation basics- Logic gates and Flip flops –Transmission Gates, TG based implementation of multiplexers, de-multiplexers, encoders, decoders, Comparator, Parity generator	**7**	15
FIRST INTERNAL TEST		

Module 3 **Memory elements:** CMOS Logic implementation of ALU, , Timer, PWM, Static and Dynamic Random Access Memory, Content Addressable Memory.	7	15
Module 4 **Analog Sub circuits**: Operational Amplifier, Inverting and Non-inverting configuration Differential Ideal amplifier basics, VCO, PLL, Comparator characteristics, two stage open loop comparator ,Switched capacitor fundamentals, Switched capacitor amplifier	**7**	15
SECOND INTERNAL TEST		
Module 5 **Digital to Analog Data Converters** : Static &Dynamic Charatersitics,1 Bit DAC, String DAC, Fully Decoded DAC,PWM DAC, Current scaling, voltage scaling DACs	7	20
Module 6 **Analog to Digital Data Converters**: Static &Dynamic Characteristics, Nyquist Criteria , Sample & Hold Circuit, Quantization error, Concept of over sampling, Counting ADC, Tracking ADC, Successive approximation ADC, Flash ADC, Dual Slope ADC. Over sampling Data Converters : Over sampling fundamentals, Delta –Sigma Converter basics, ∑ Modulator.	7	20

Assessment procedure

i) Two internal tests, each having 15%
ii) Tutorials/Assignments/ Mini projects having 10%
iii) End Semester examination having 60%

07 EC 7405: SEMINAR

Credits: 0-0-2: 2 **Year: 2015**

Prerequisite: Nil

Course Objectives : This course is intended for

- Increasing the breadth of knowledge
- Enhancing the ability of self study
- Improving presentation and communication skills
- Augmenting the skill of Technical Report Writing.

Course Outcomes:

The graduate will have acquired

- Debating capability and presentation skills in a technical topic of his interest.
- Knowledge about contemporary issues and research opportunities
- Capacity to communicate effectively and professionally in both verbal and written forms
- Capability for self education and lifelong learning

Outline and Evaluation procedure:

Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 30 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students. Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.

Internal continuous assessment : 100 marks

Marks for the report: 30%
Presentation: 40%
Ability to answer questions on the topic: 30%

07 EC 7407: MASTERS RESEARCH PROJECT (PHASE I)

Teaching scheme: 12 hours per week **Credits:** 6

Course objectives*:*

- To identify current issues in the area of Embedded Systems.
- To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes.
- The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

. **Course Outcomes:**

The graduate will have acquired

- Knowledge about contemporary issues and research opportunities
- Capacity to communicate effectively and professionally in both verbal and written forms
- Capability of self education and lifelong learning
- Understanding of professional and ethical responsibility

Outline and Evaluation procedure:

The project work should be a project in Embedded system stream. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential, they may be permitted to do their project outside the parent institute subject to the conditions in clause 10 of M.Tech regulations. Department will constitute an Evaluation Committee to review the project work. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

The student is required to undertake the masters research project phase-Iduring the third semester and the same is continued in the 4th semester.(Phase-II).Phase-I consists of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4thsemester.

Internal continuous assessment : 50 marks

Progress evaluation by the Project Supervisor : 20 Marks

Presentation and evaluation by the committee : 30 Marks

SEMESTER 4

07 EC 7402: MASTERS RESEARCH PROJECT (PHASE II)

Teaching scheme: 21 hours per week **Credits:** 12

Course Objectives:

- To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes.
- The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

Course Outcomes:

The graduate will have acquired

- Knowledge about contemporary issues and research opportunities
- Capacity to communicate effectively and professionally in both verbal and written forms
- Capability of self education and lifelong learning
- Understanding of professional and ethical responsibility

Outline and Evaluation procedure:

Masters Research project phase-II is a continuation of project phase-Istarted in the third semester. Before the end of the fourth semester, there will be two reviews, one at middle of the fourth semester and other towards the end. In the first review, progress of the project work done is to be assessed. In the second review, the complete assessment (quality, quantum and authenticity) of the Thesis is to be evaluated. Both the reviews should be conducted by guide and Evaluation committee. This would be a pre qualifying exercise for the students for getting approval for the submission of the thesis. At least one technical paper is to be prepared for possible publication in journal or conferences. The technical paper is to be submitted along with the thesis. The final evaluation of the project will be external evaluation.

Project Progress evaluation details: Marks:100

Internal continuous assessment : 70 marks

Extenal assessment : 30 marks

Project evaluation by the supervisor/s : 30 Marks

Presentation & evaluation by the Committee : 40 Marks

Evaluation by the External expert : 30 Marks